Digitizing the Analog World: Challenges and Opportunities

April 5, 2010

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Murmann Mixed-Signal Group

STANFORD ELECTRICAL ENGINEERING

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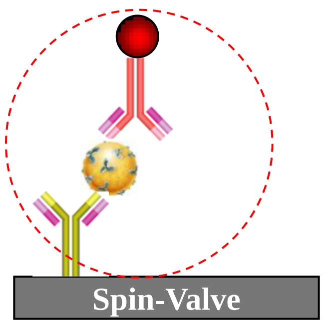
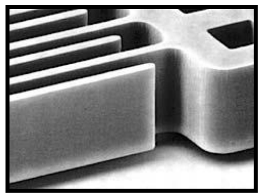
Research Overview

Biomolecule detection

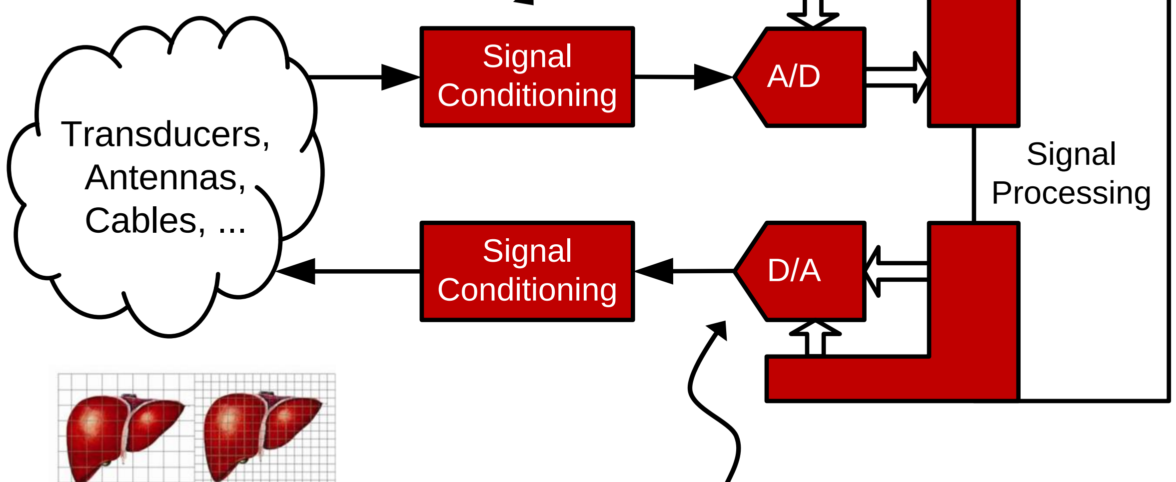


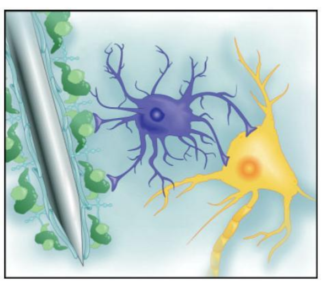
MEMS



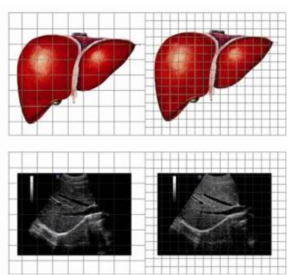
Sensor interfaces

Digital enhancement algorithms





Neural prosthetics



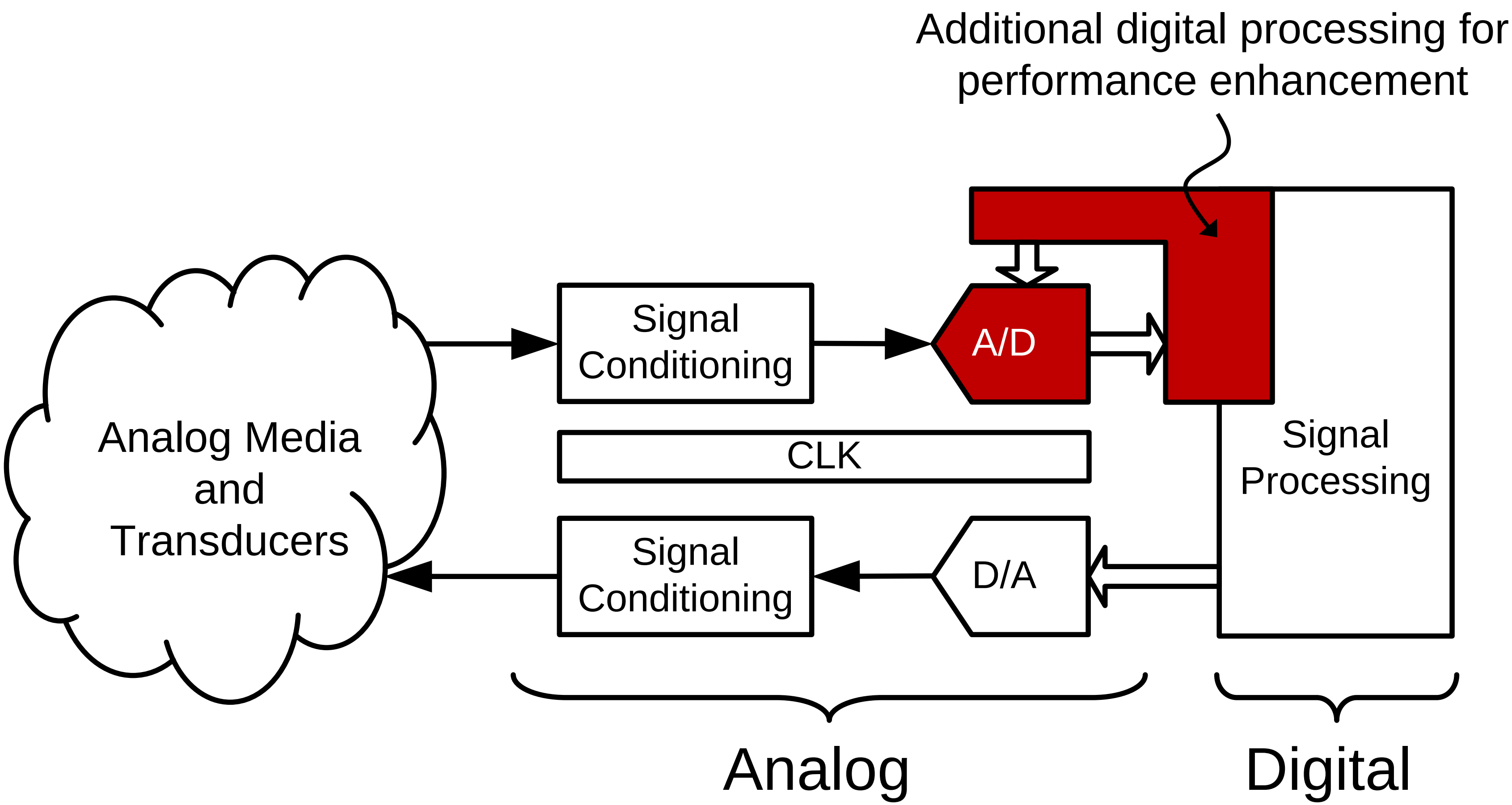
Medical ultrasound

High-performance and low-power A/D and D/A converters

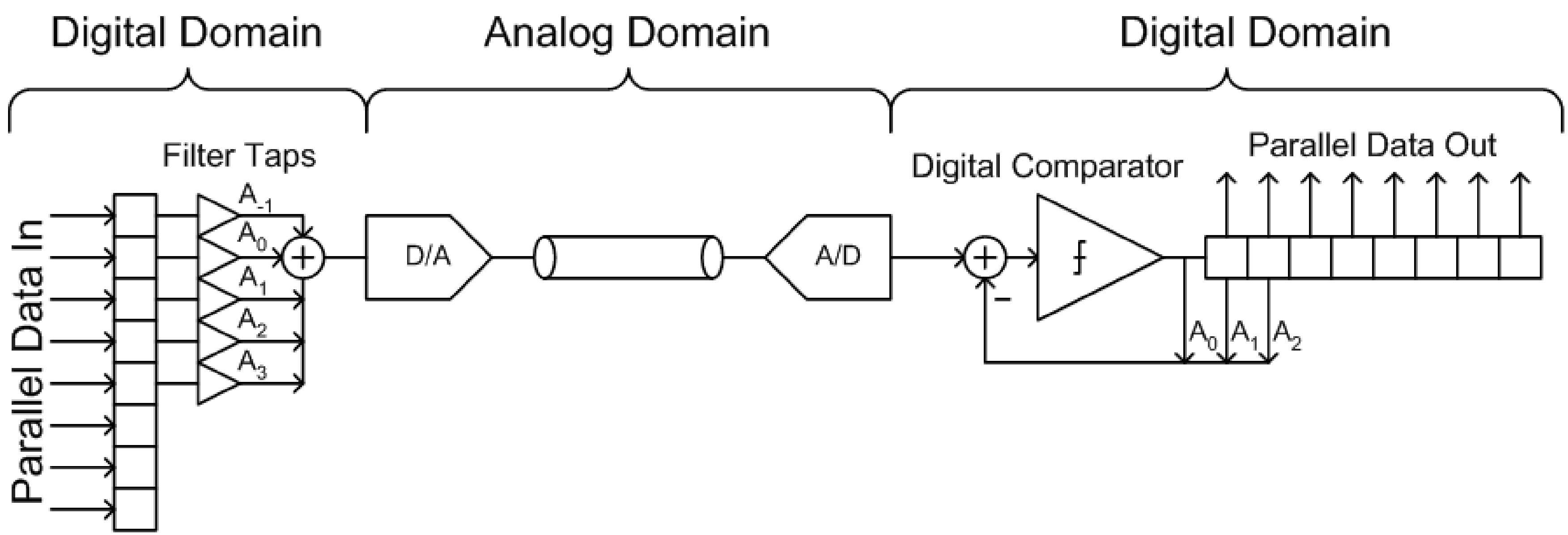
Research Examples

- High-performance A/D converters
- Neural prosthetics
- MEMS accelerometers
- Large area electronics

Digitally Assisted A/D Converters



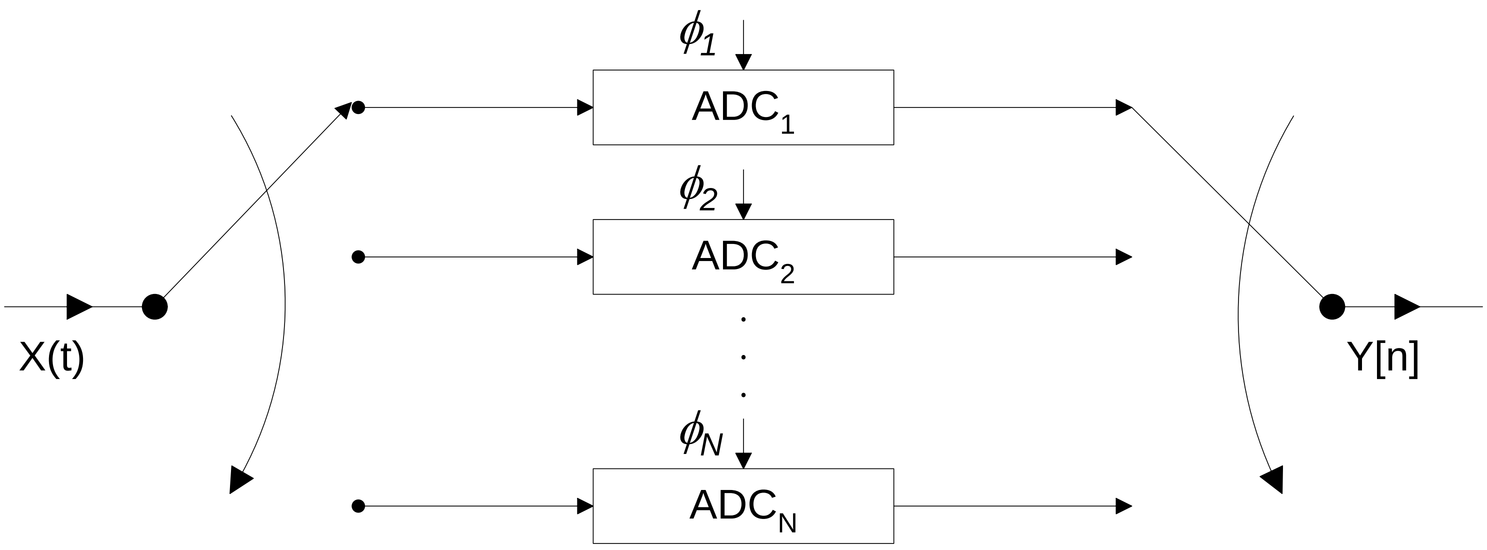
ADC for a "Digital" Serial Link



- No analog error accumulation and better scalability
- Need efficient high-speed ADC, typically > 10GS/s

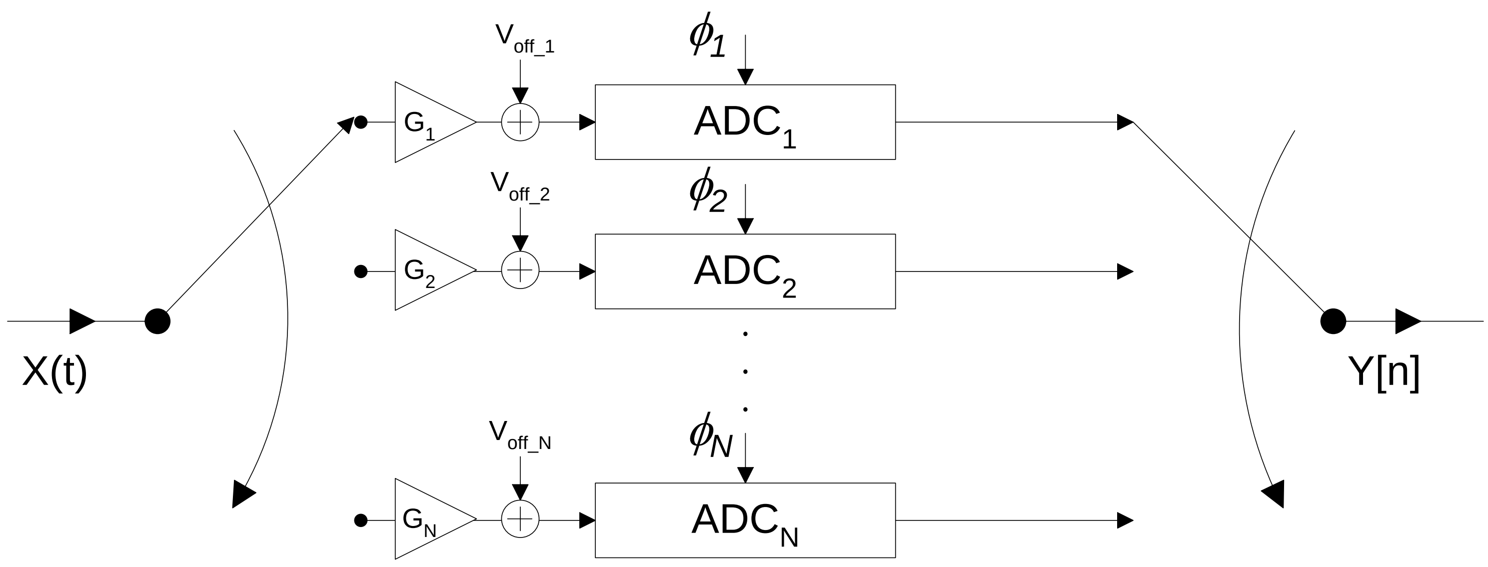
Time-Interleaving

- Popular way to increase ADC throuhgput



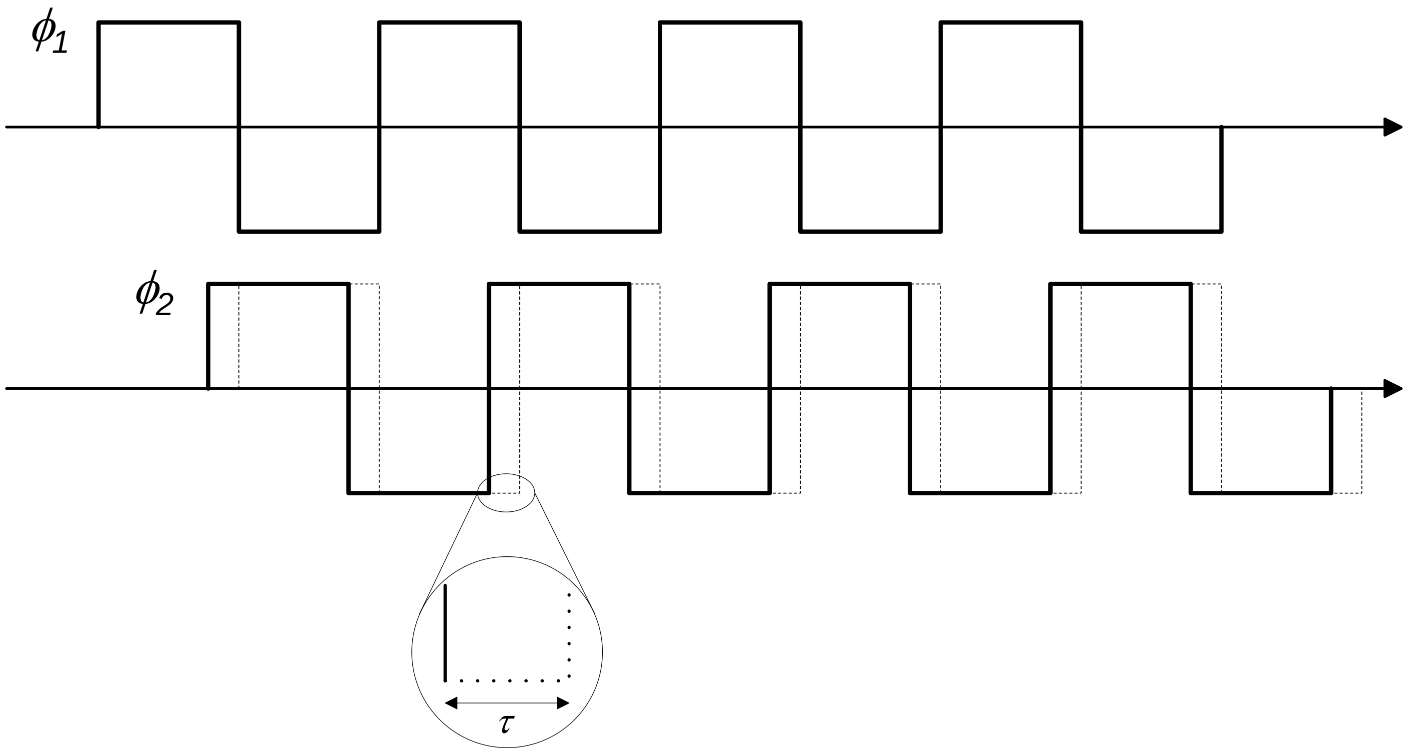
Imperfections

- Mismatches result in signal distortion
  - Gain
  - Offset
  - Timing Skew



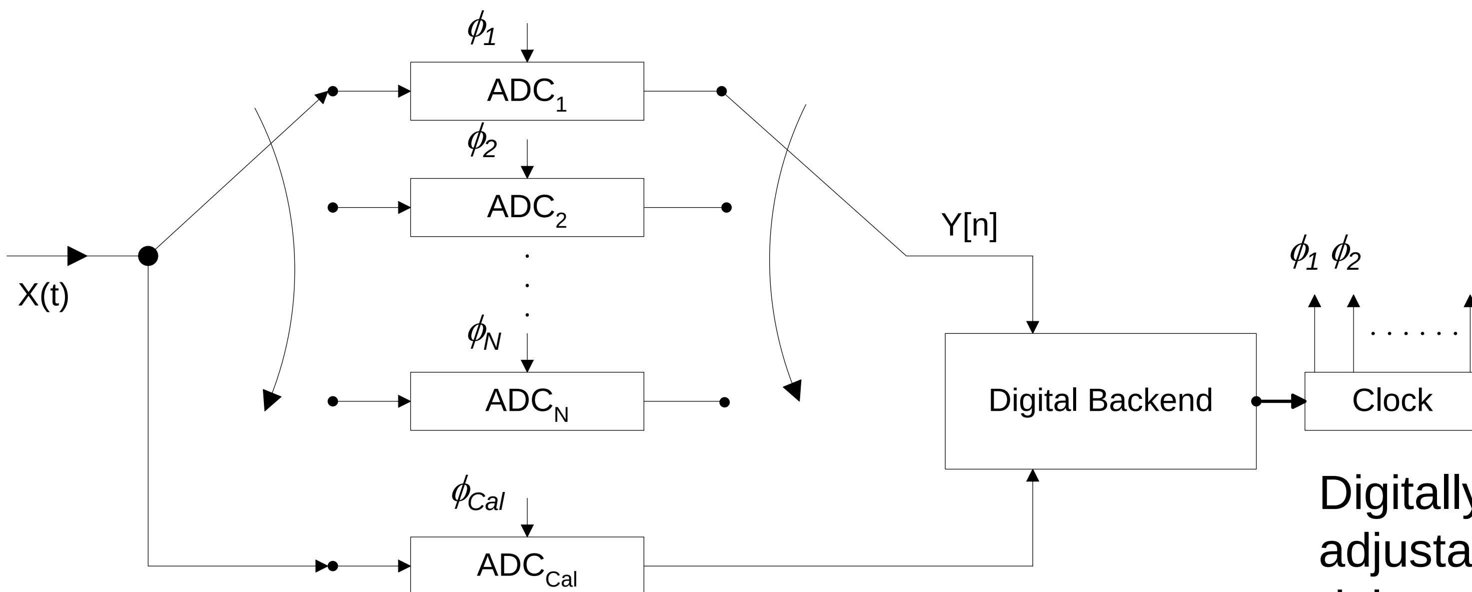
Our Focus: Timing Skew

(2-channel example)



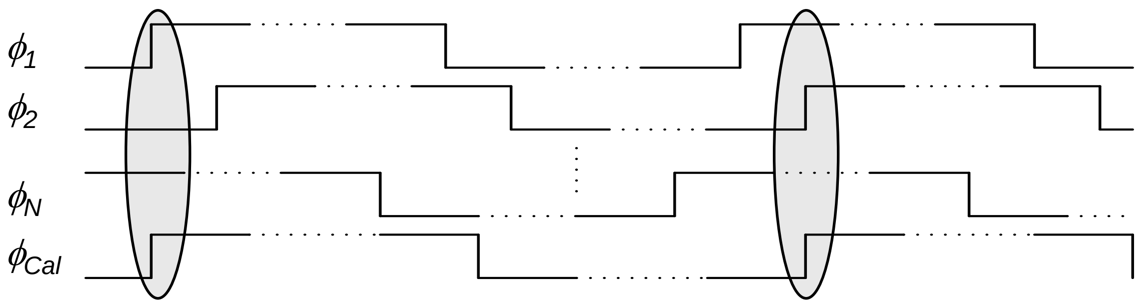
Skew Calibration Using Extra ADC

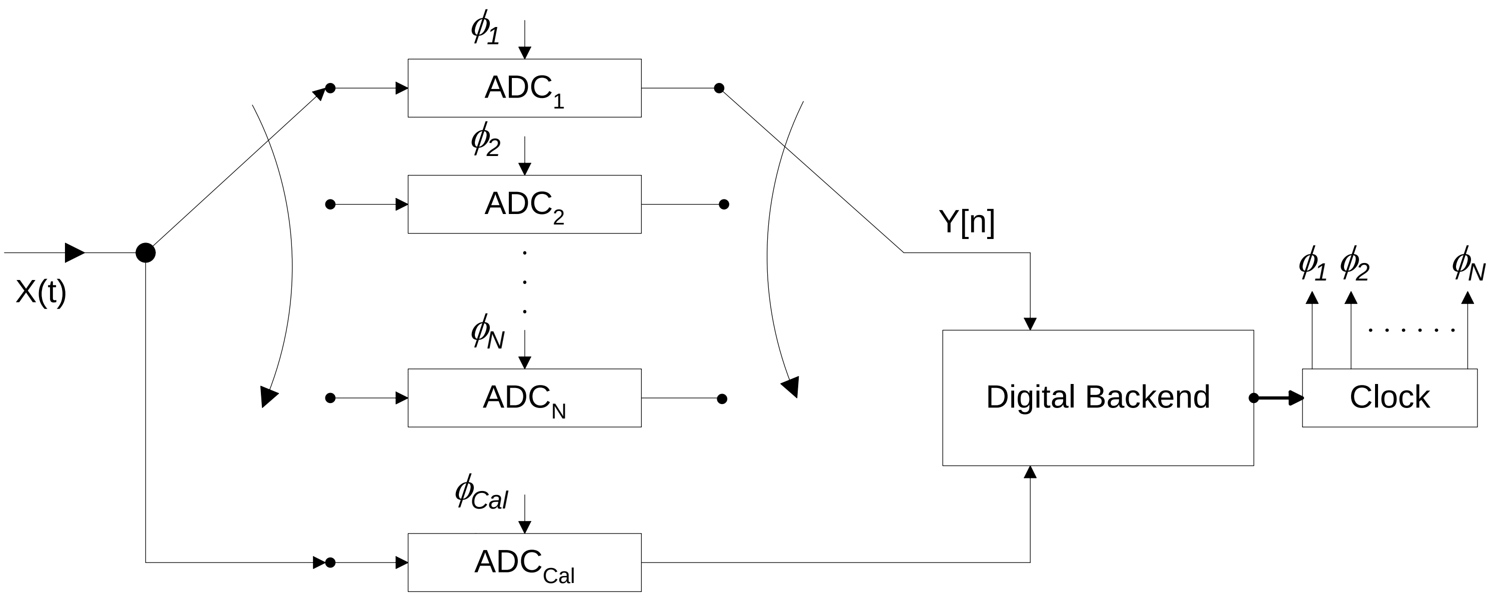
- Statistics-based skew measurement in digital backend
- Correction through analog adjustments



Digitally adjustable delay cells

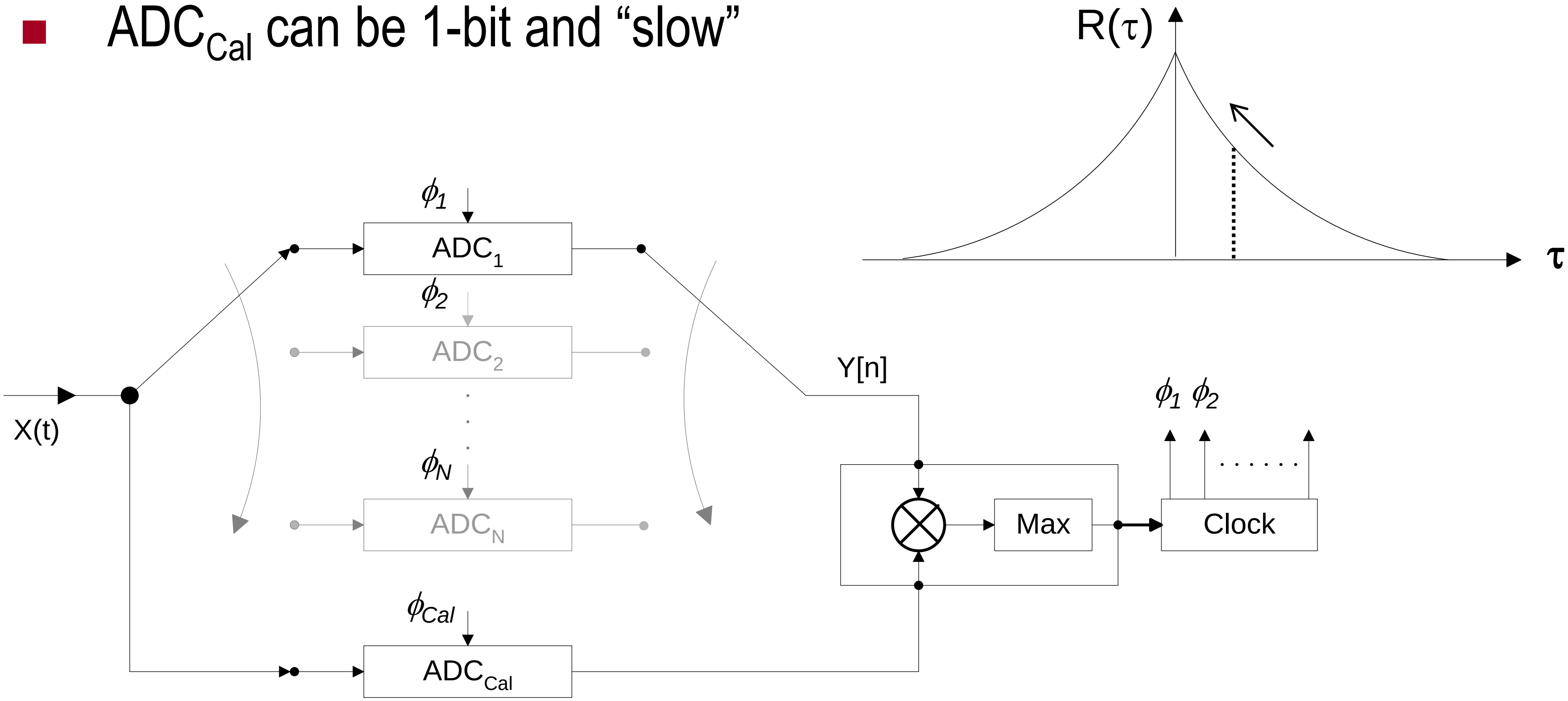
Timing of Auxiliary ADC Phase





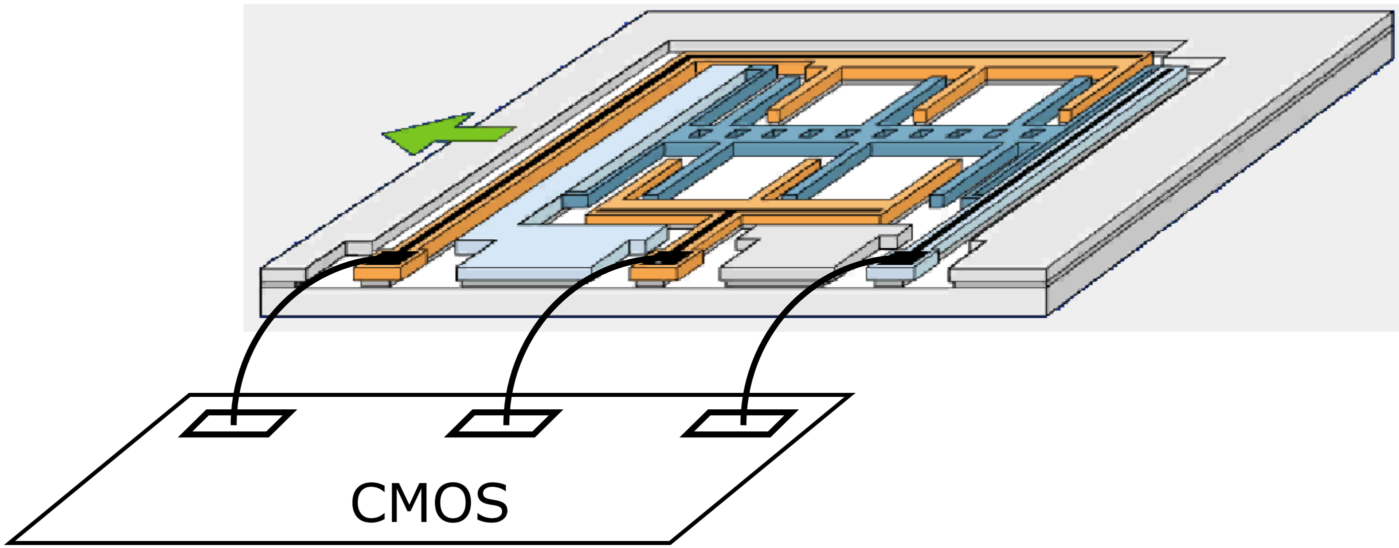
Calibration Scheme

- For each channel, adjust delay cells until correlation between calibration ADC output and each slice are maximized
- ADC_{Cal} can be 1-bit and “slow”



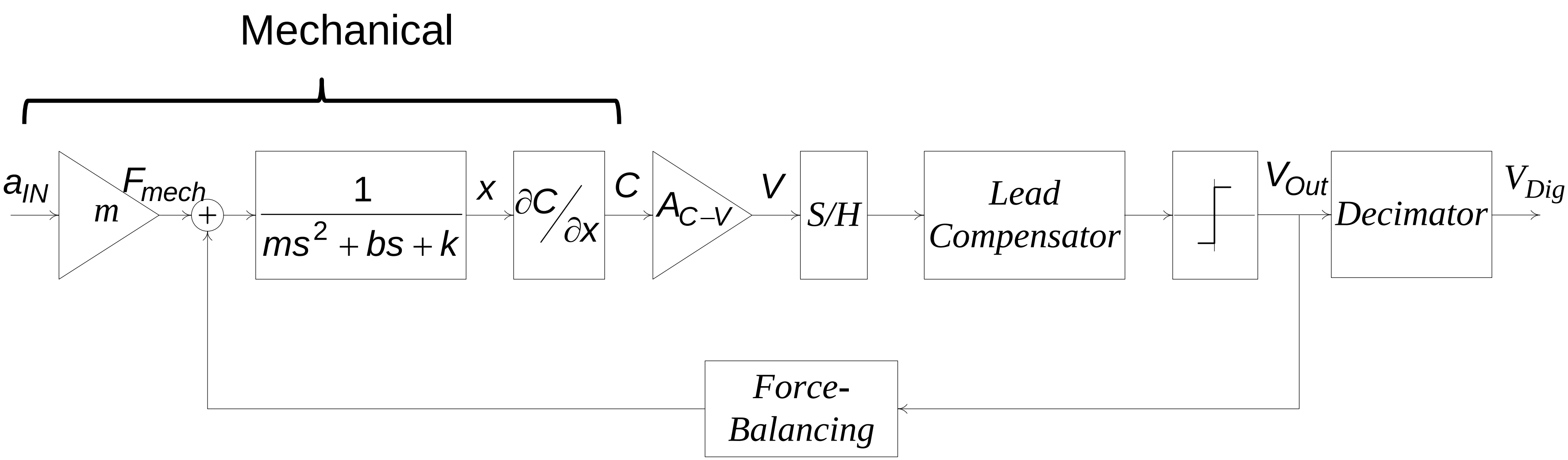
- Removed pre-publication slides on experimental results…

MEMS Accelerometer



- Capacitance change ~10 fF/g
- Desired resolution ~10 mg for airbags and ESP
  - Must resolve capacitance changes of ~100 aF
- Problem: Drift in parasitic bondwire capacitance

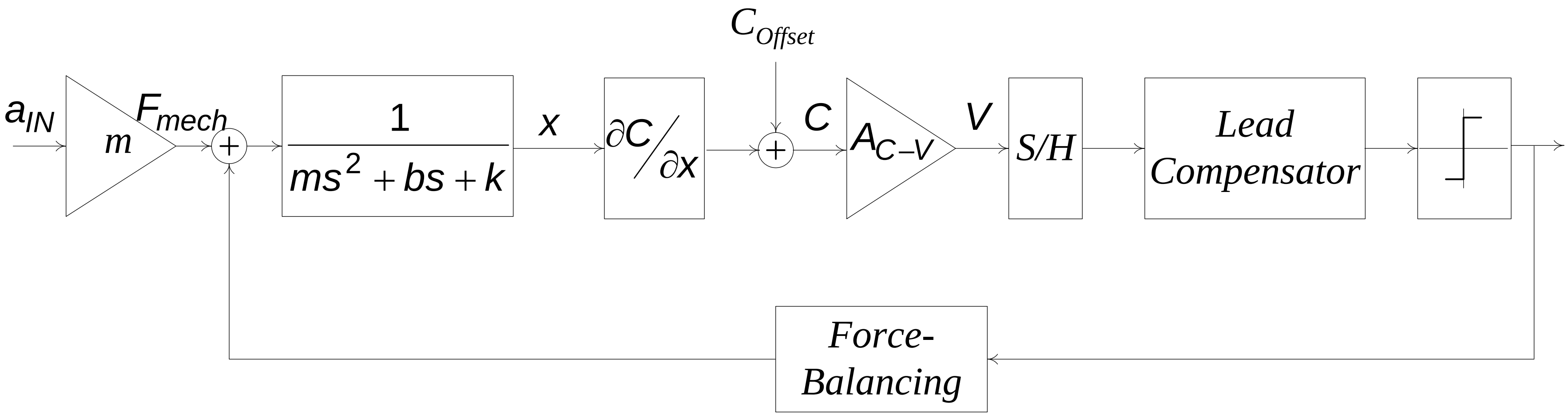
Sigma-Delta Interface



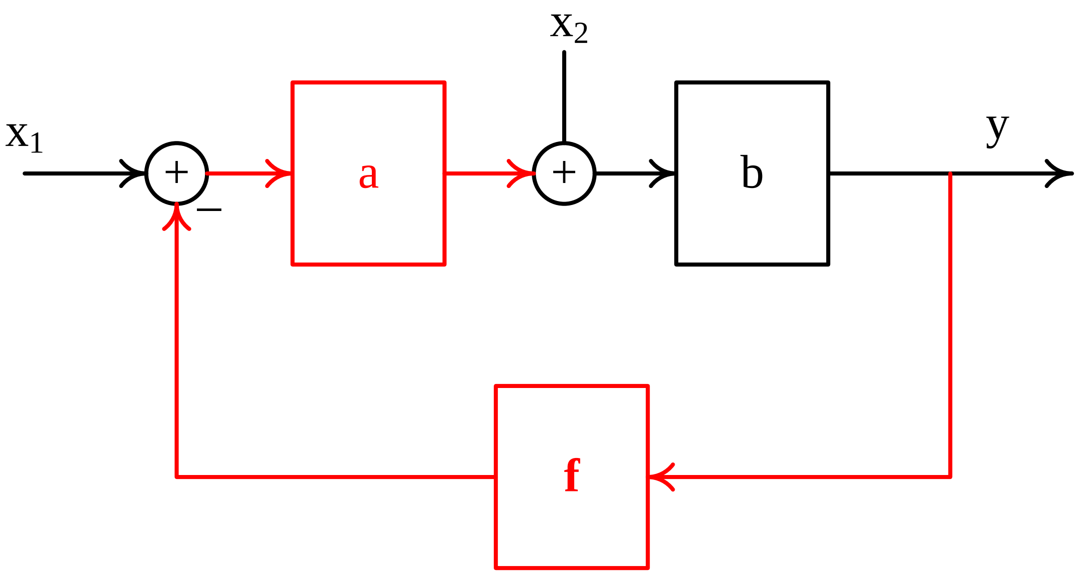
M. Lemkin and B. E. Boser, "A three-axis micromachined accelerometer with a CMOS position-sense interface and digital offset-trim electronics," *IEEE J. Solid-State Circuits*, vol. 34, pp. 456-468, April 1999.

Offset

Offset due to bond wire deformation



Linear Feedback System with Two Inputs

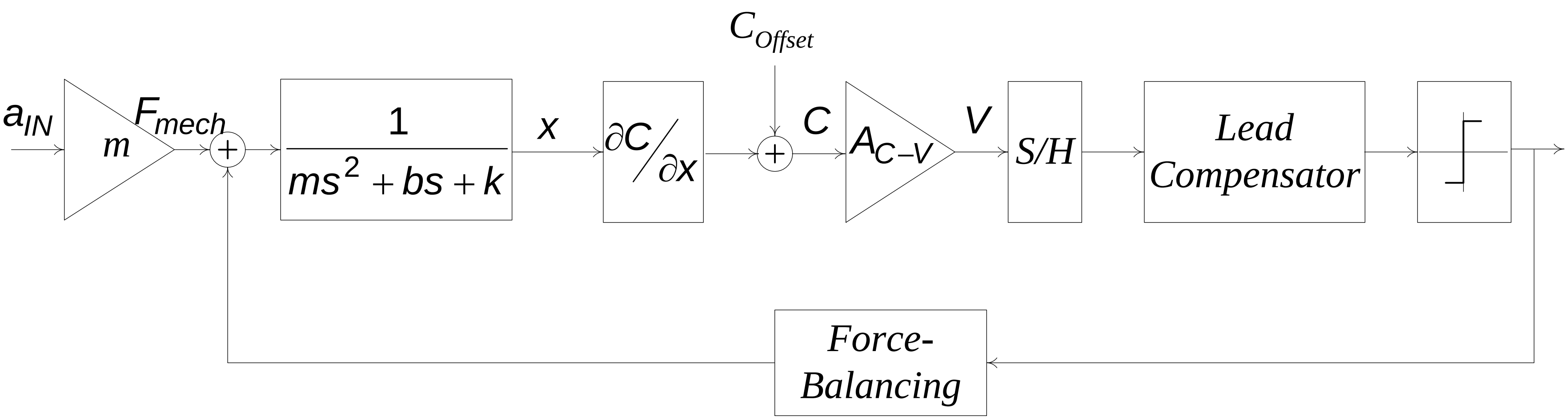


$$y \cong x_1 \cdot \frac{1}{f} + x_2 \cdot \frac{1}{af}$$

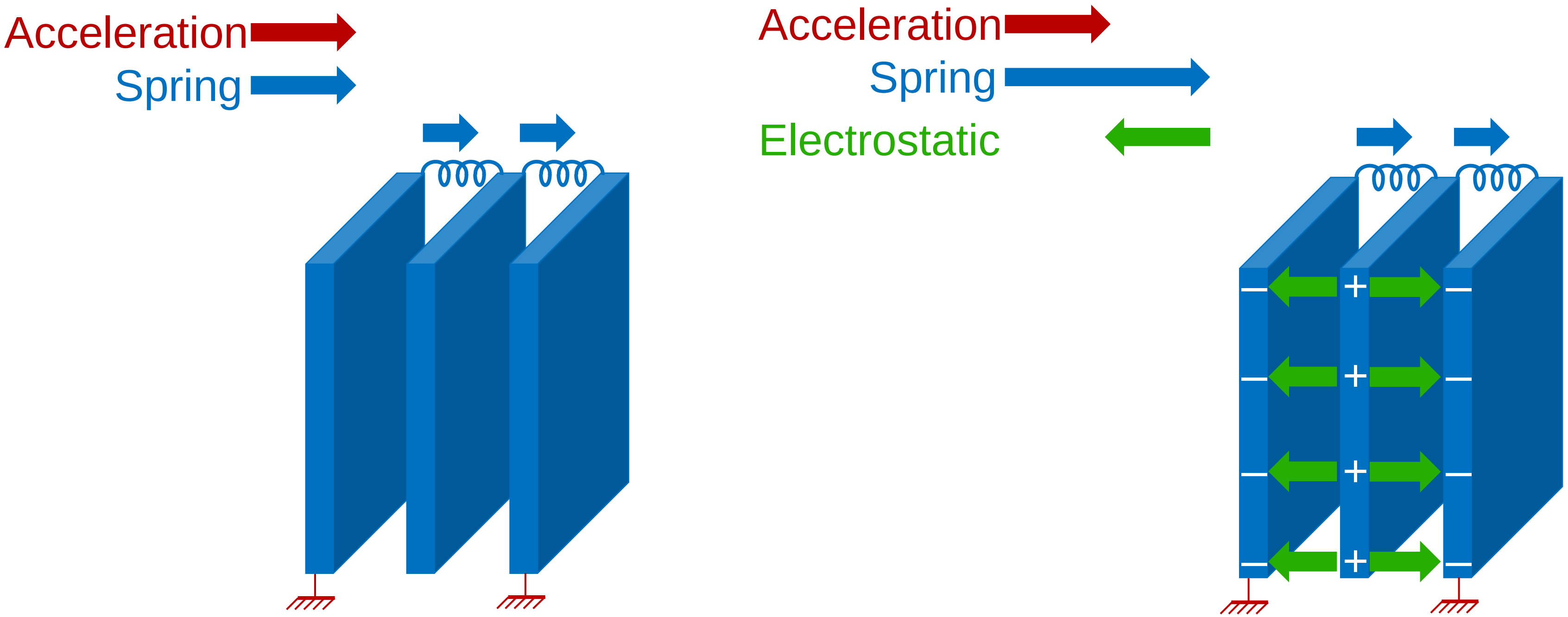
Spring Constant Modulation

- The output due to C_{off} can be modulated to higher frequencies by modulating the spring constant k

$$V_{Out} \cong F_{mech} \cdot \frac{1}{FB} + C_{Off} \cdot \frac{k + \tilde{k}}{FB \cdot \frac{\partial C}{\partial x}}$$

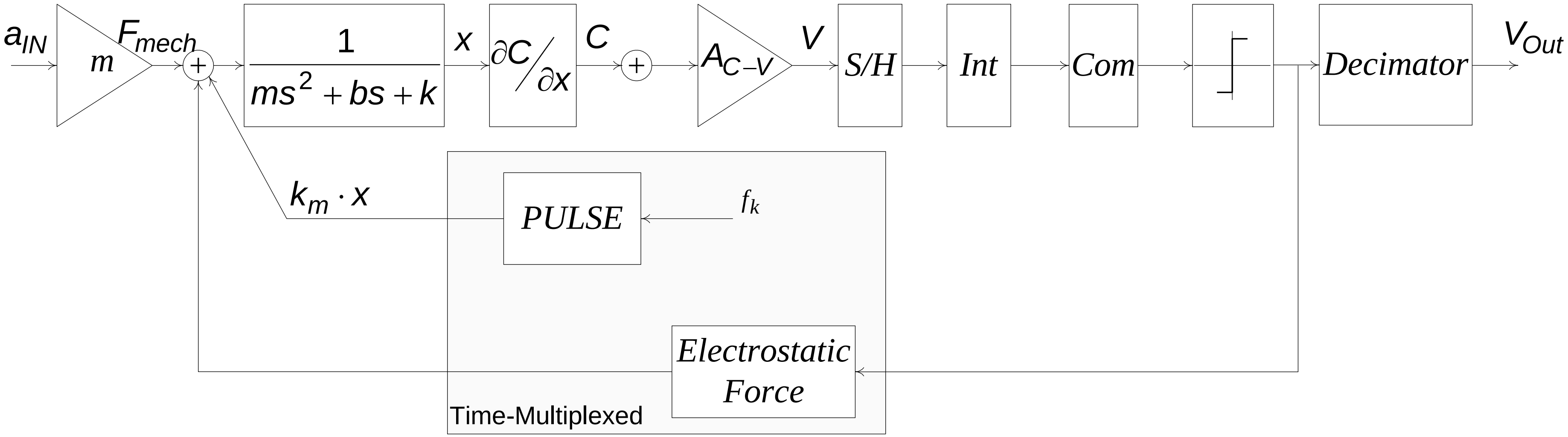


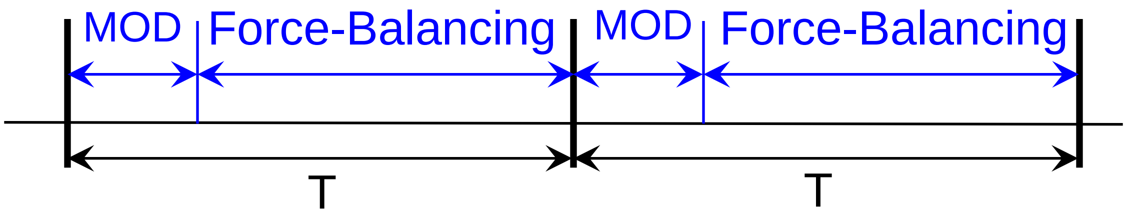
Spring softening effect



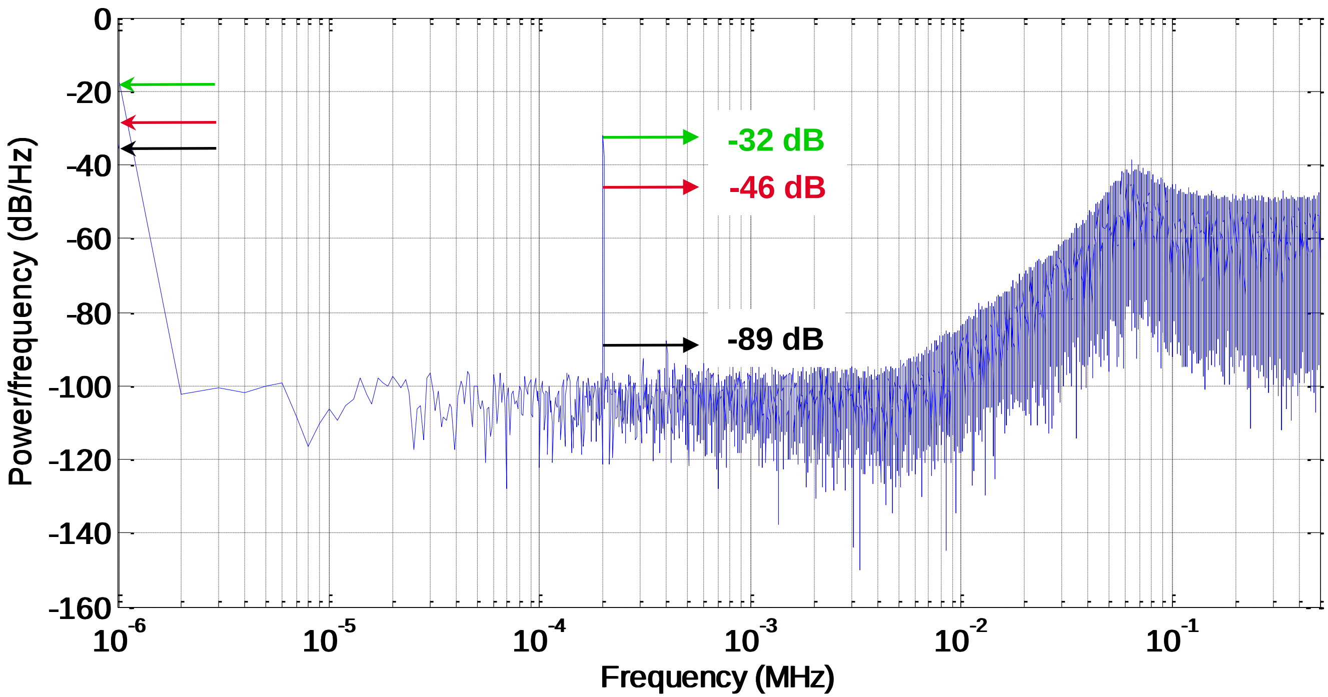
- Can be used to modulate spring constant (k)

Modulation through Multiplexed Feedback

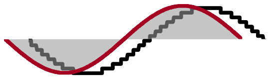




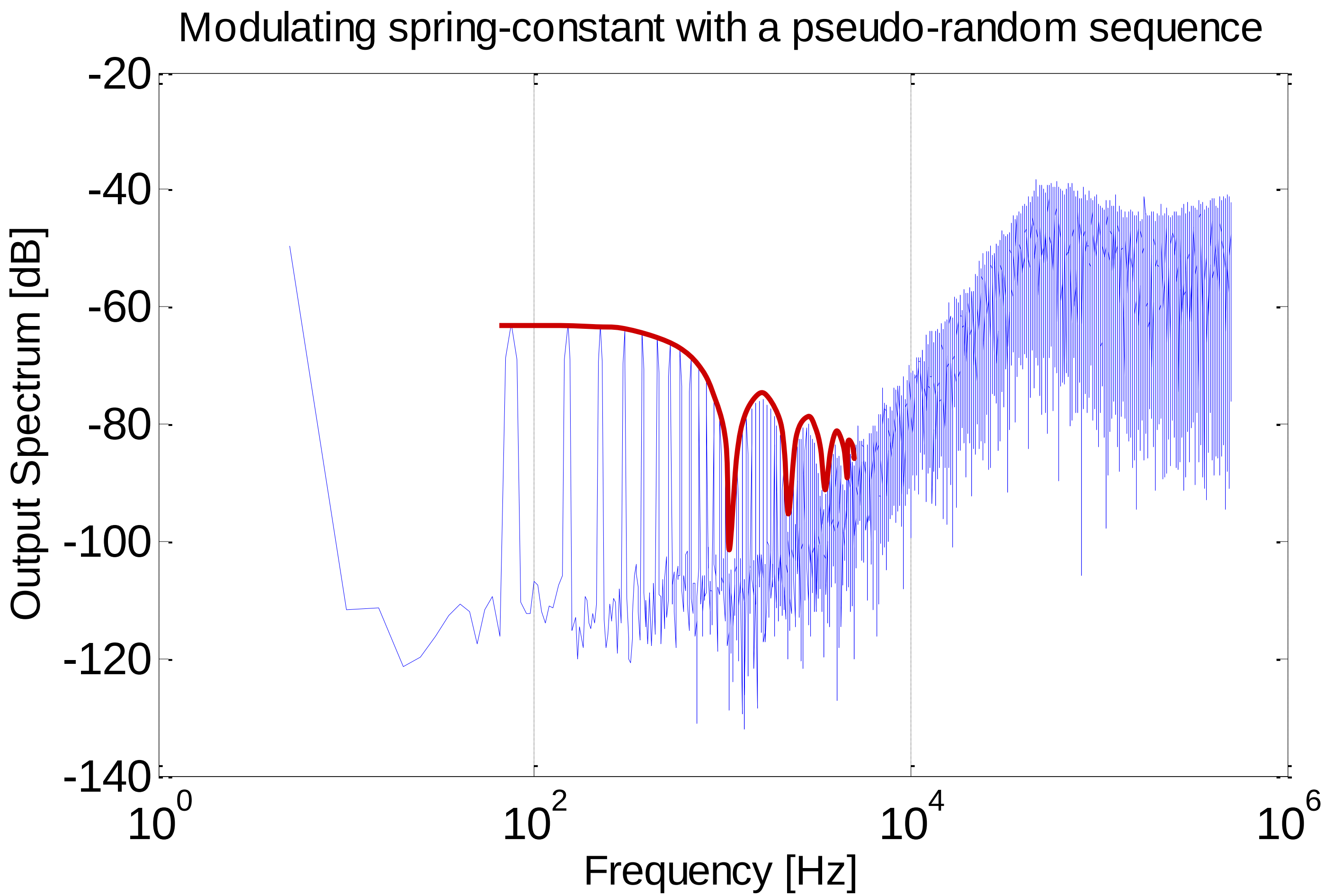
Output Spectrum with 1-Tone Modulation



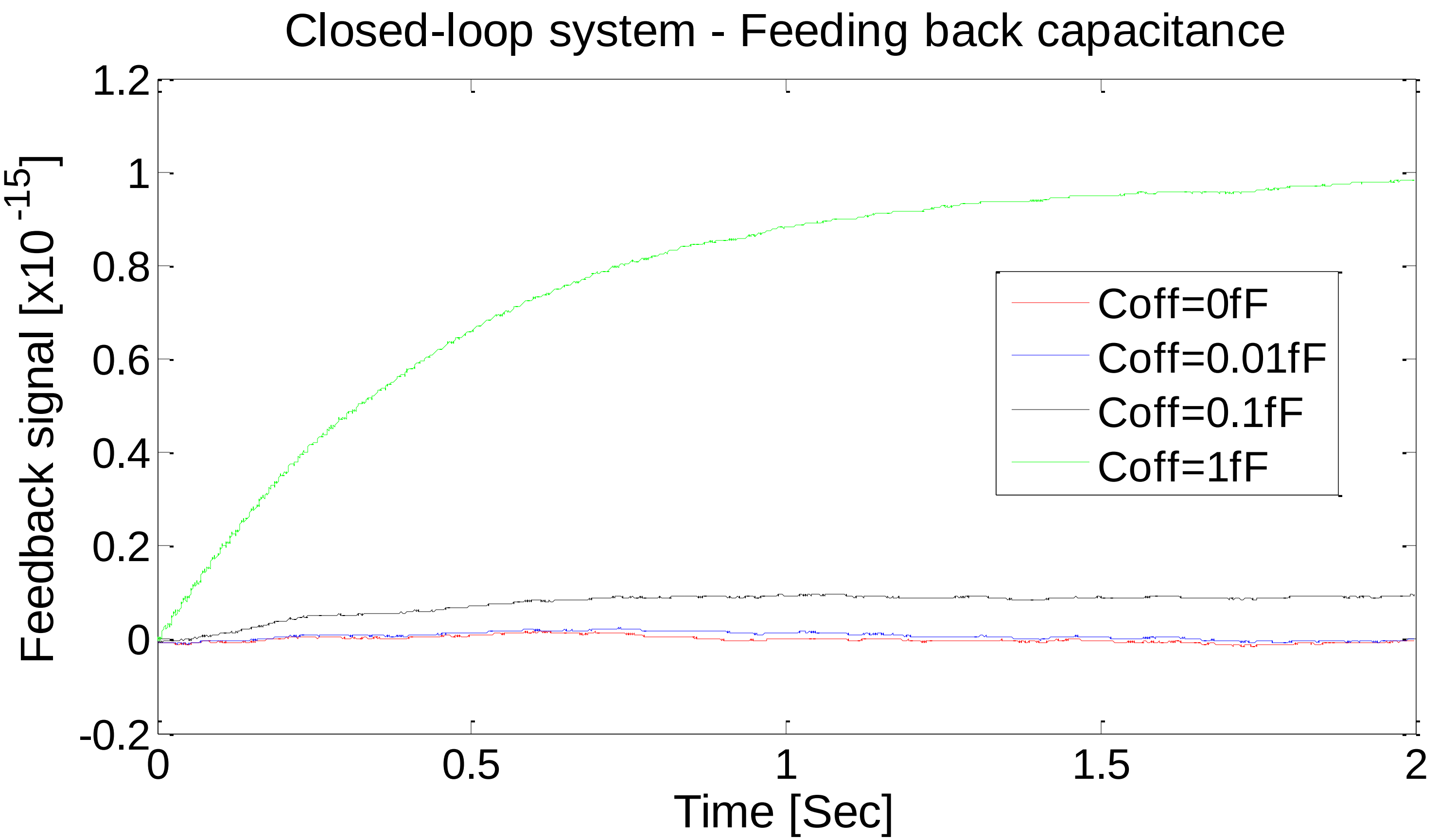
DC Acceleration	Offset Capacitance
9.1 m/s^2	**0 fF**
9.1 m/s^2	**10 fF**
9.1 m/s^2	**50 fF**



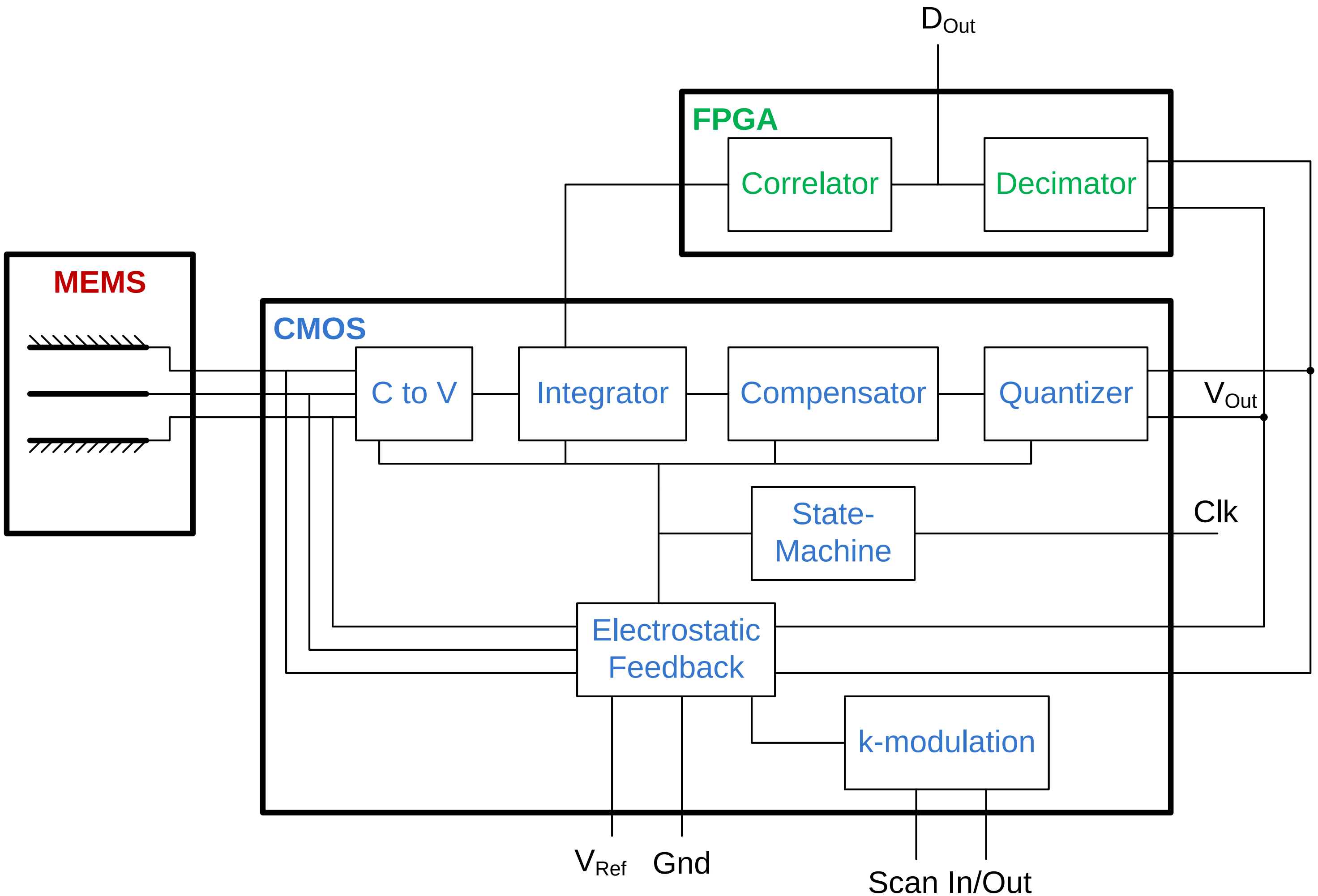
Pseudo-Random Modulation



Parameter Convergence

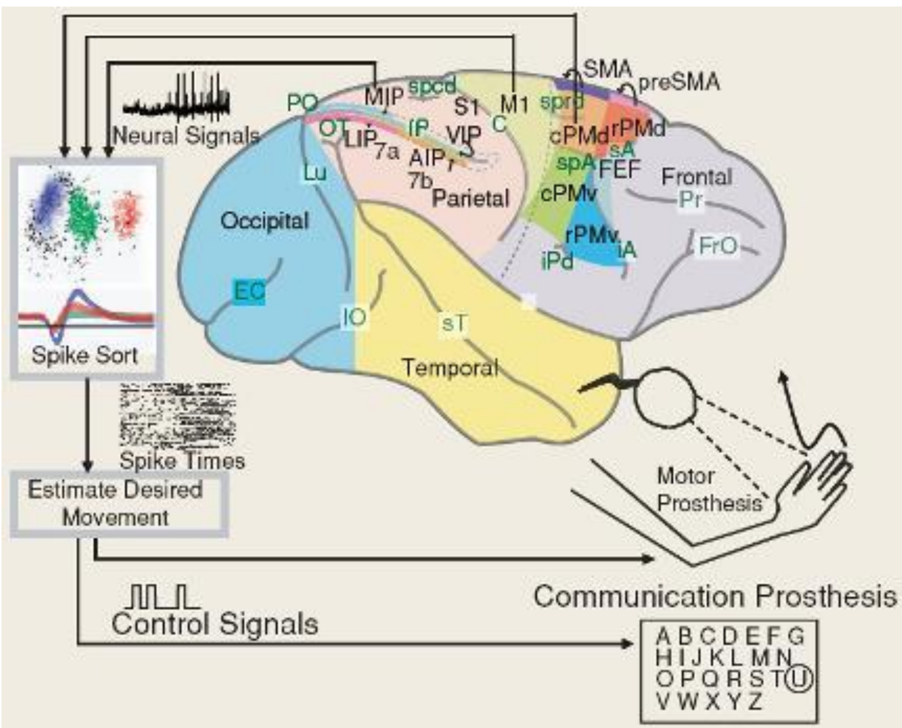


Chip Design in Progress

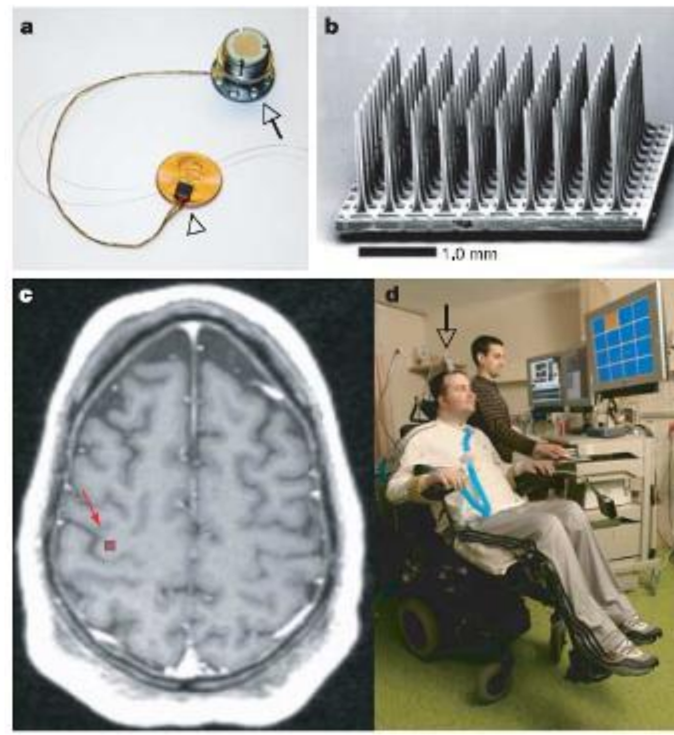


Neural Prosthetics

- Cortical motor prosthetics
  - Neurons in the motor cortical areas of the brain encode information about intended movement



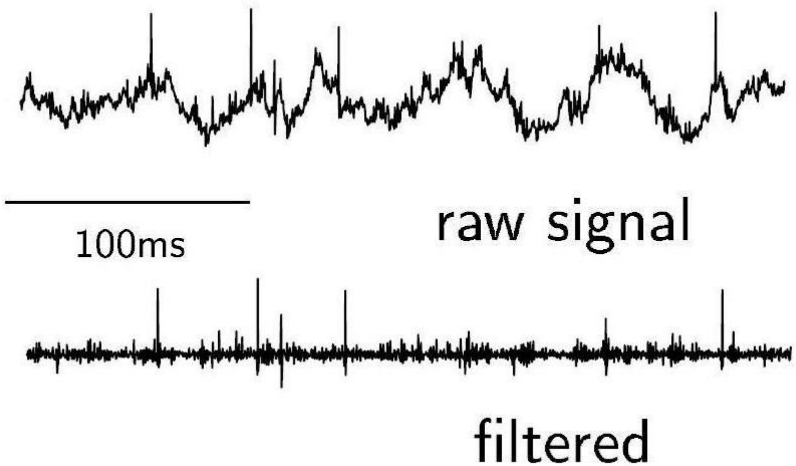
Courtesy K.V. Shenoy



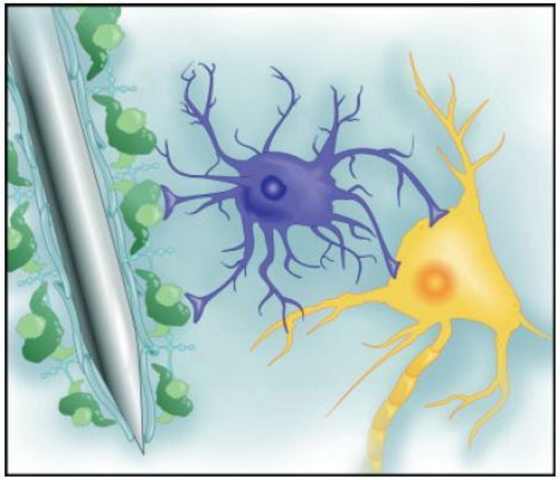
Courtesy L.R. Hochberg
Nature Magazine June ‘06

Neural Signal Acquisition

- Electrode signals consist of multiple sources
  - DC Offset, about 15mV from electrode/tissue interface
  - Local field potential (LFP), ≤3mV peak, 10Hz to 100Hz
  - Spikes from nearby neurons, 35µV – 1mV peak, 500Hz to 5kHz



Courtesy M. Sahani



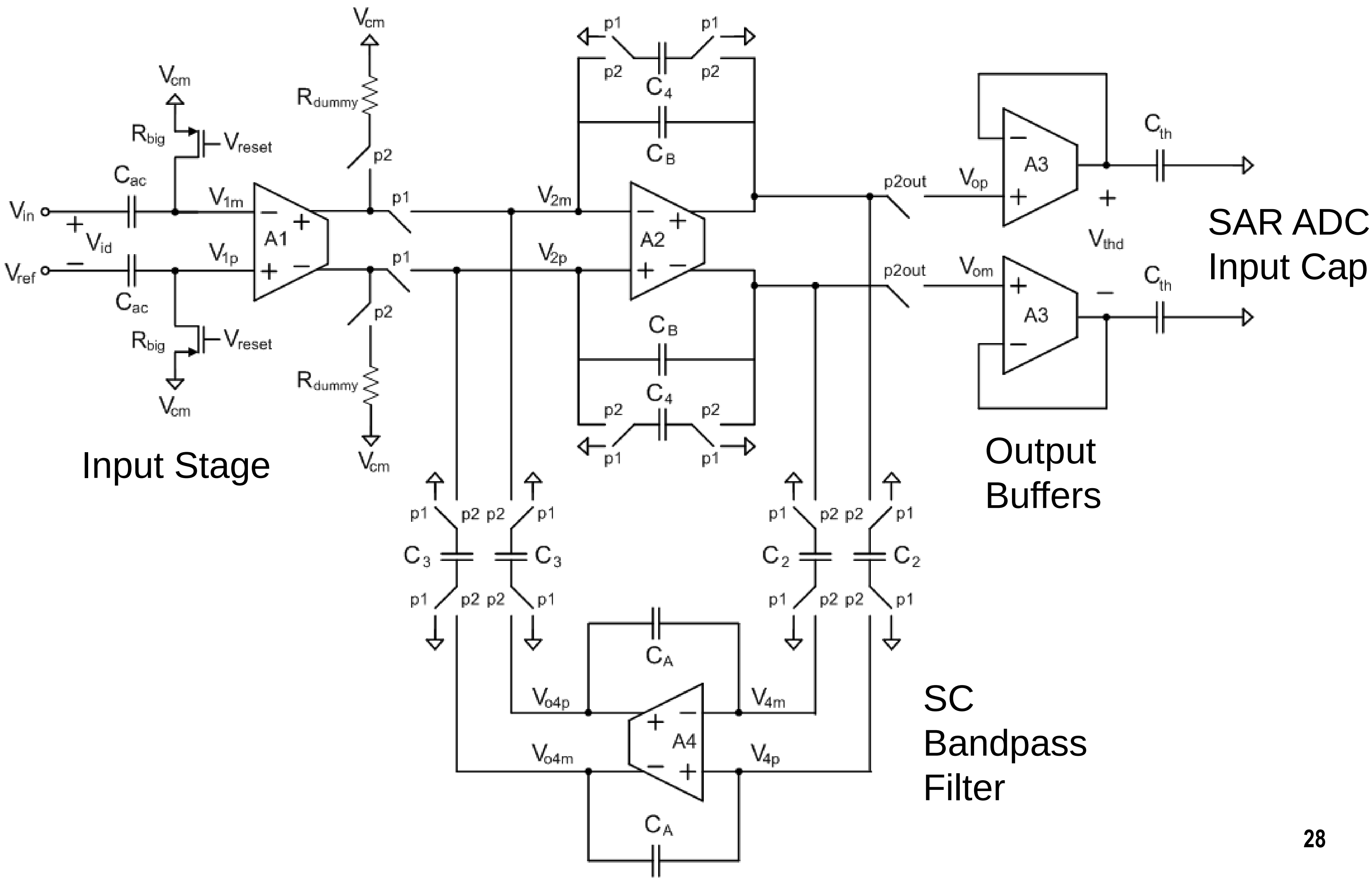
Courtesy C.L. Klaver

Specs

- Separate the fast and slow signal acquisition for DR
  - Custom front end design for each path

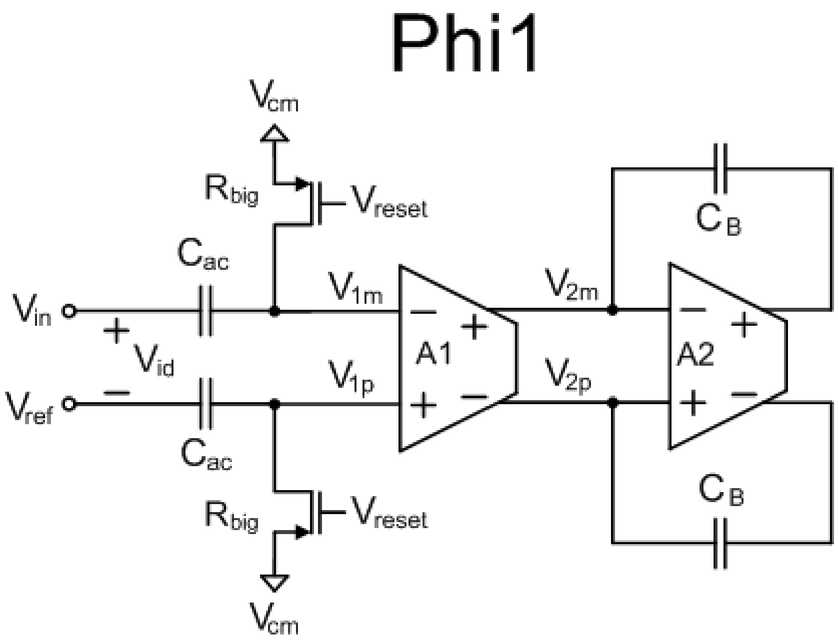
	Spikes	Local Field Potential
Gain	600 V/V	200 V/V
Lower Cutoff	300Hz	1Hz
Upper Cutoff	10kHz	1kHz
Input Referred Noise (total from sampling node)	2.0μVrms	1.0μVrms in 10-100Hz
Total Power (96x Array)	3mW	100μW

Spike Path Front-End

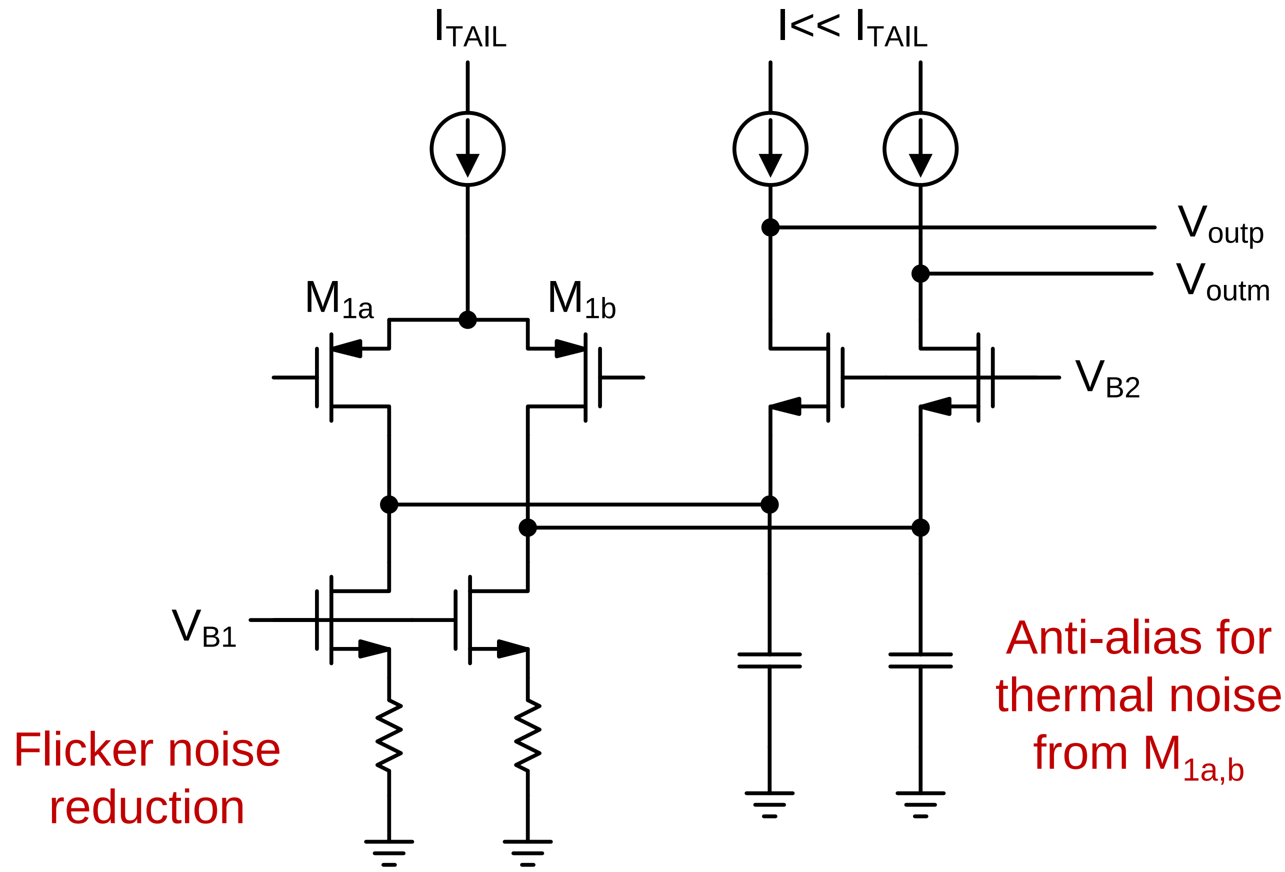


Sampling Phase

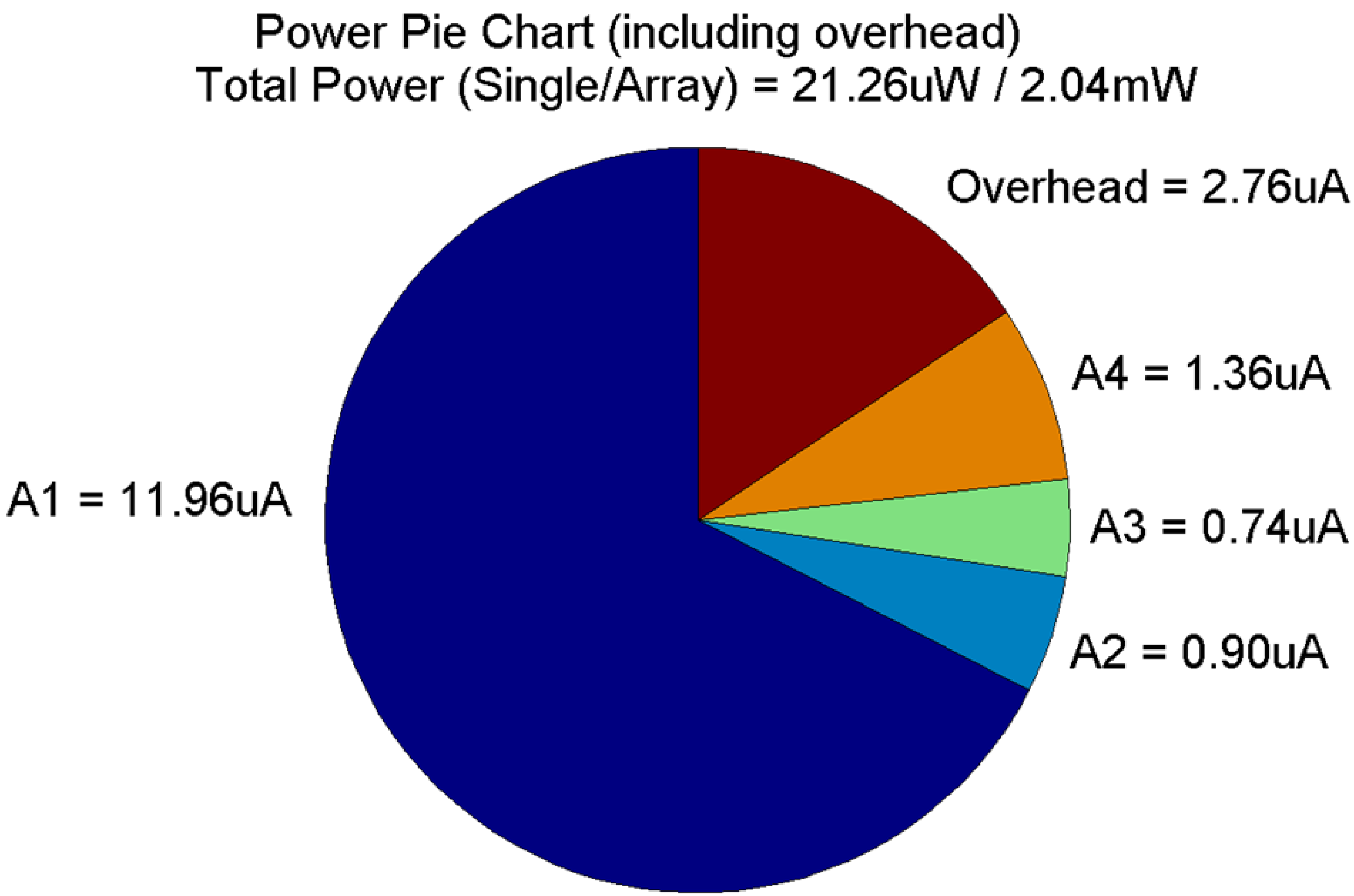
- Integrate signal current on C_B and sample
  - High-pass for DC block using C_{ac} and R_{big} (off-resistance)
  - A_1 contains a pole that helps minimize noise folding



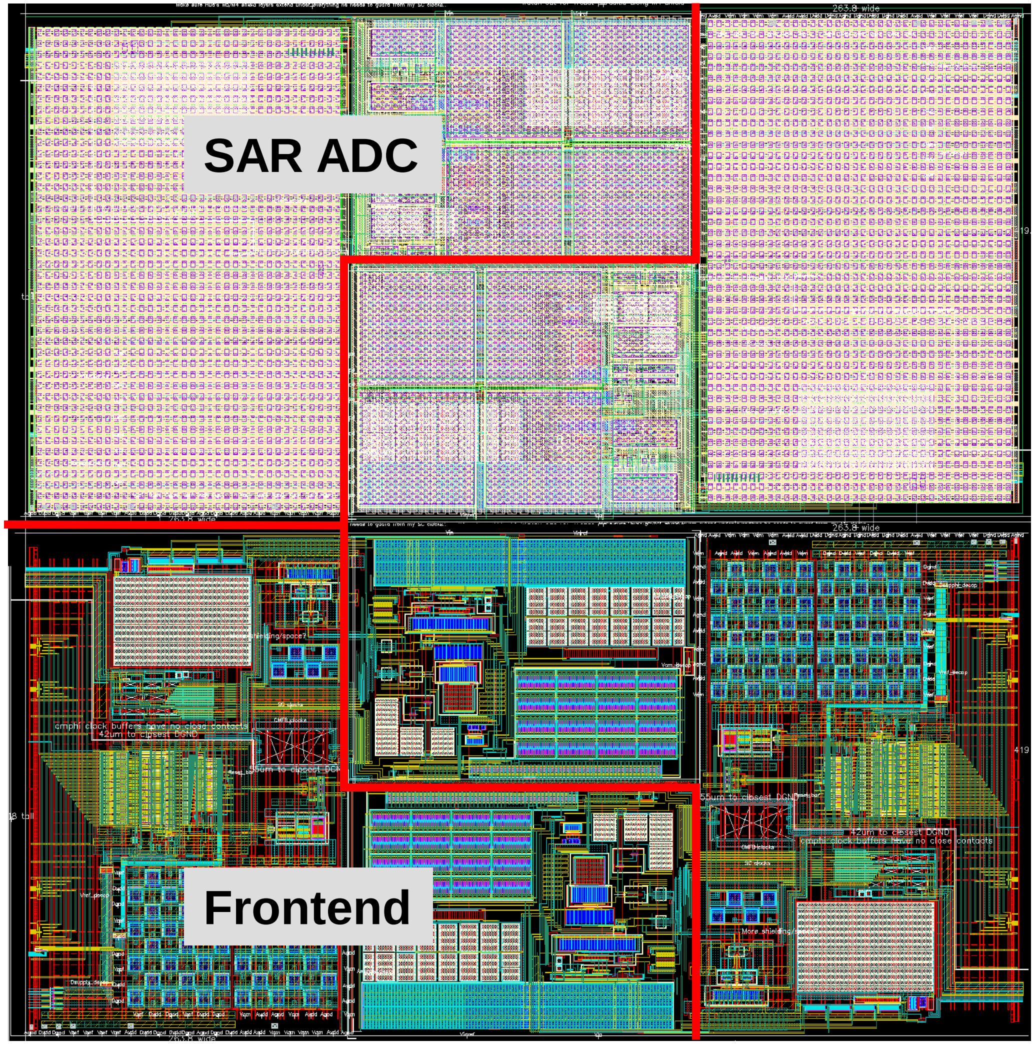
A1 Implementation Details



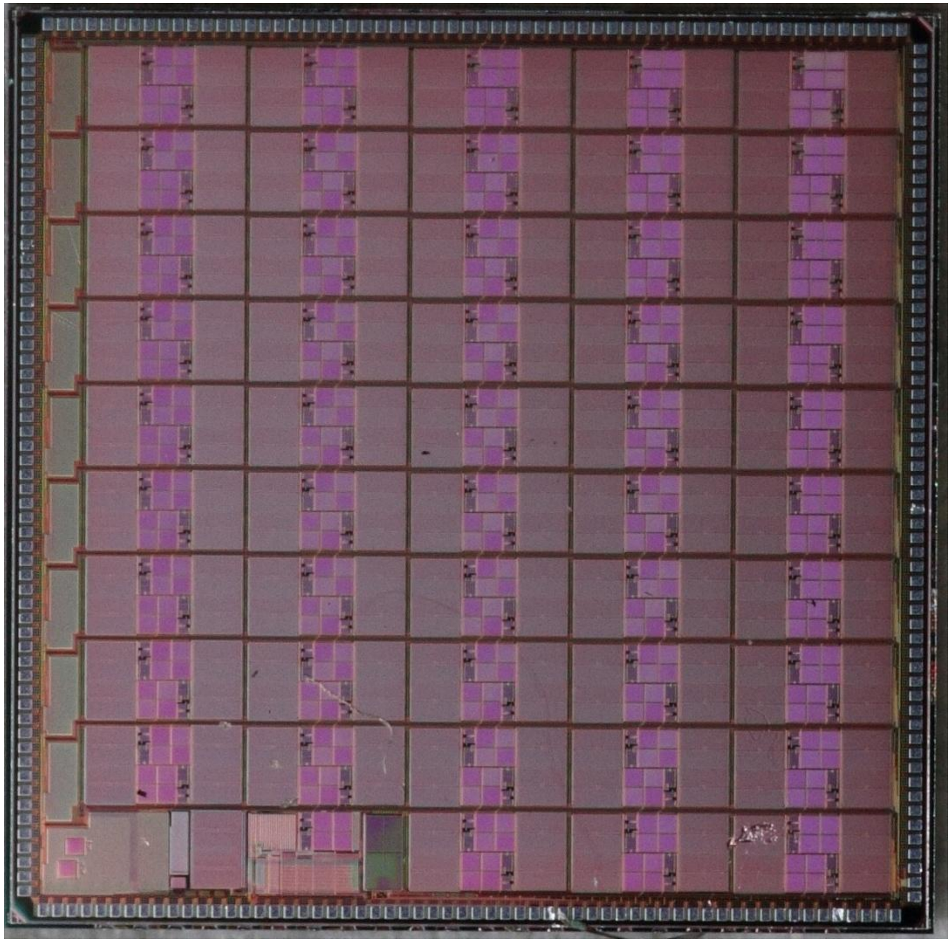
Static Power



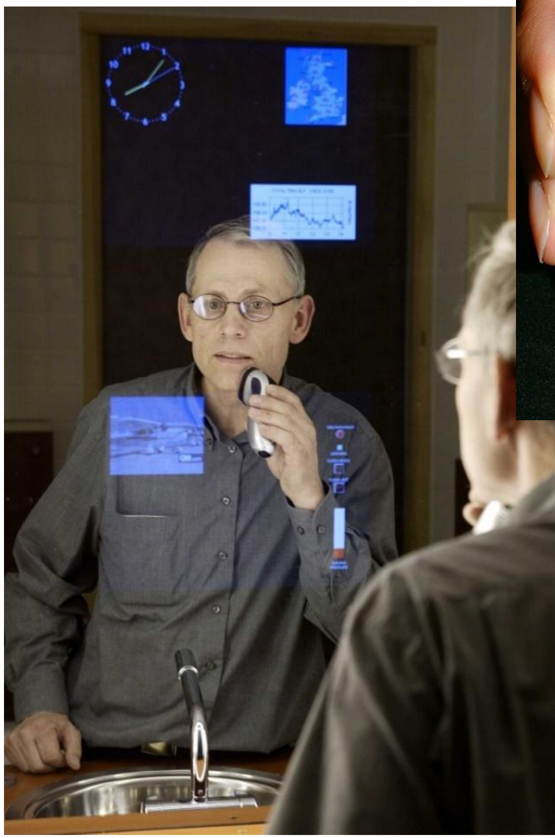
Two-Channel Interface Pixel

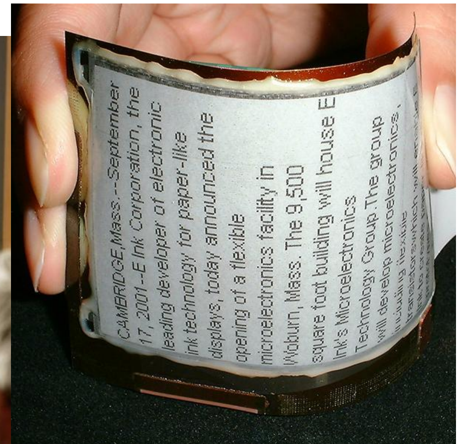


Die Photo (96 channels, 5mm x 5mm)



The Future?




CAMBRIDGE,Mass.--September
17, 2001--E Ink Corporation, the
leading developer of electronic
ink technology for paper-like
displays, today announced the
opening of a flexible
microelectronics facility in
Woburn, Mass. The 9,500
square foot building will house E
Ink's Microelectronics
Technology Group.The group
will develop microelectronics,


29%
PAYMENT CARD
27%
TIP
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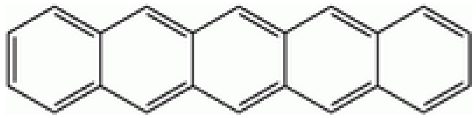
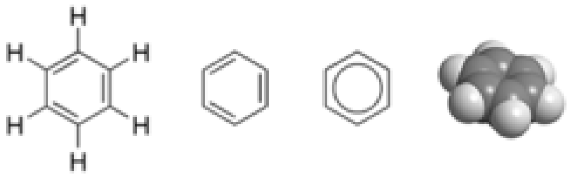
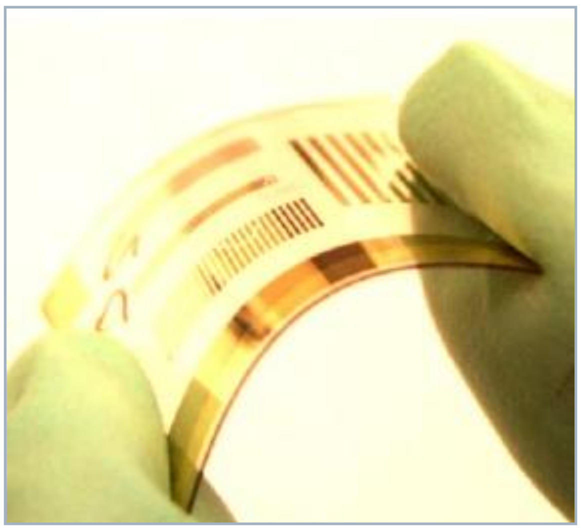
engadget

Organic Semiconductors



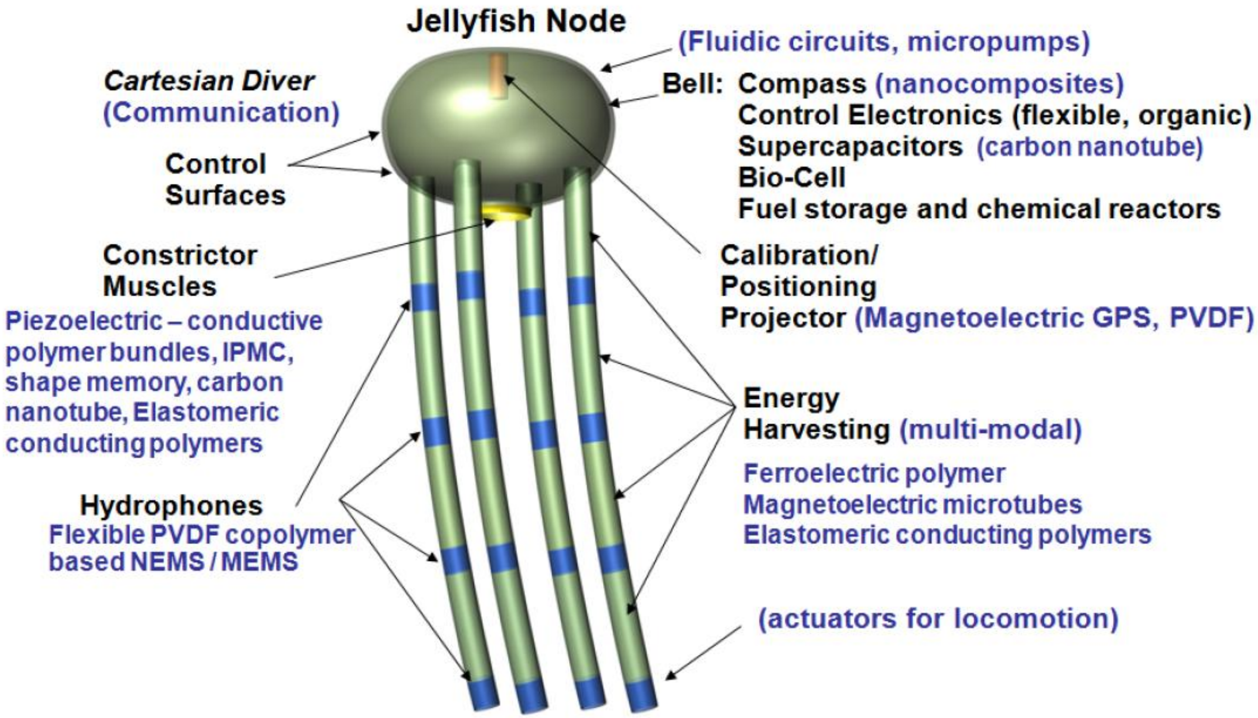


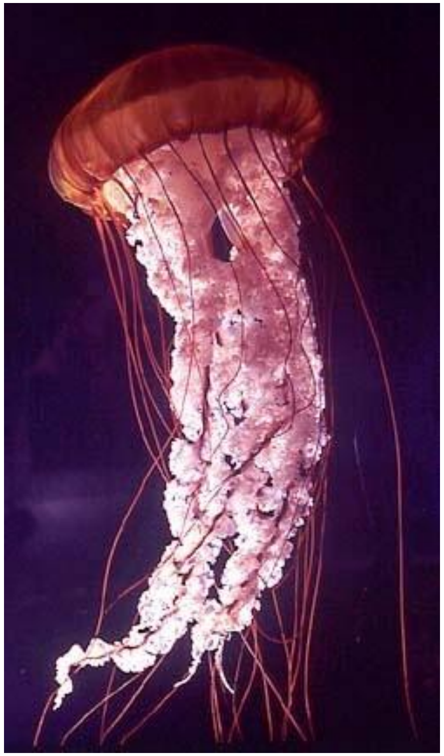
- Mechanically flexible
- Suitable for solution processing
  - Cover large areas at low cost
  - Make disposable devices



M. Berggren, D. Nilsson, and N. D. Robinson, Nat. Mater. **6**, (2007).

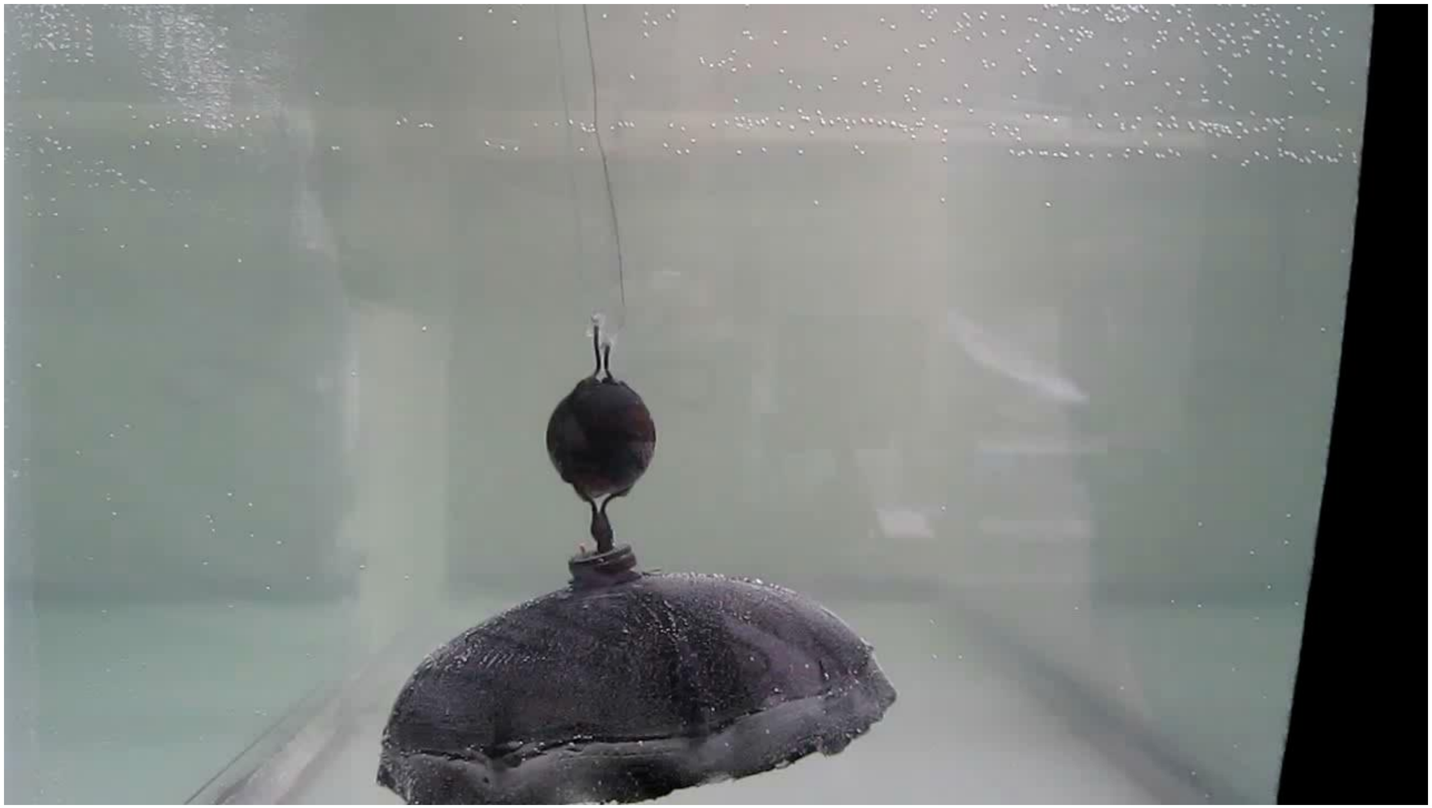
Jellyfish Autonomous Node





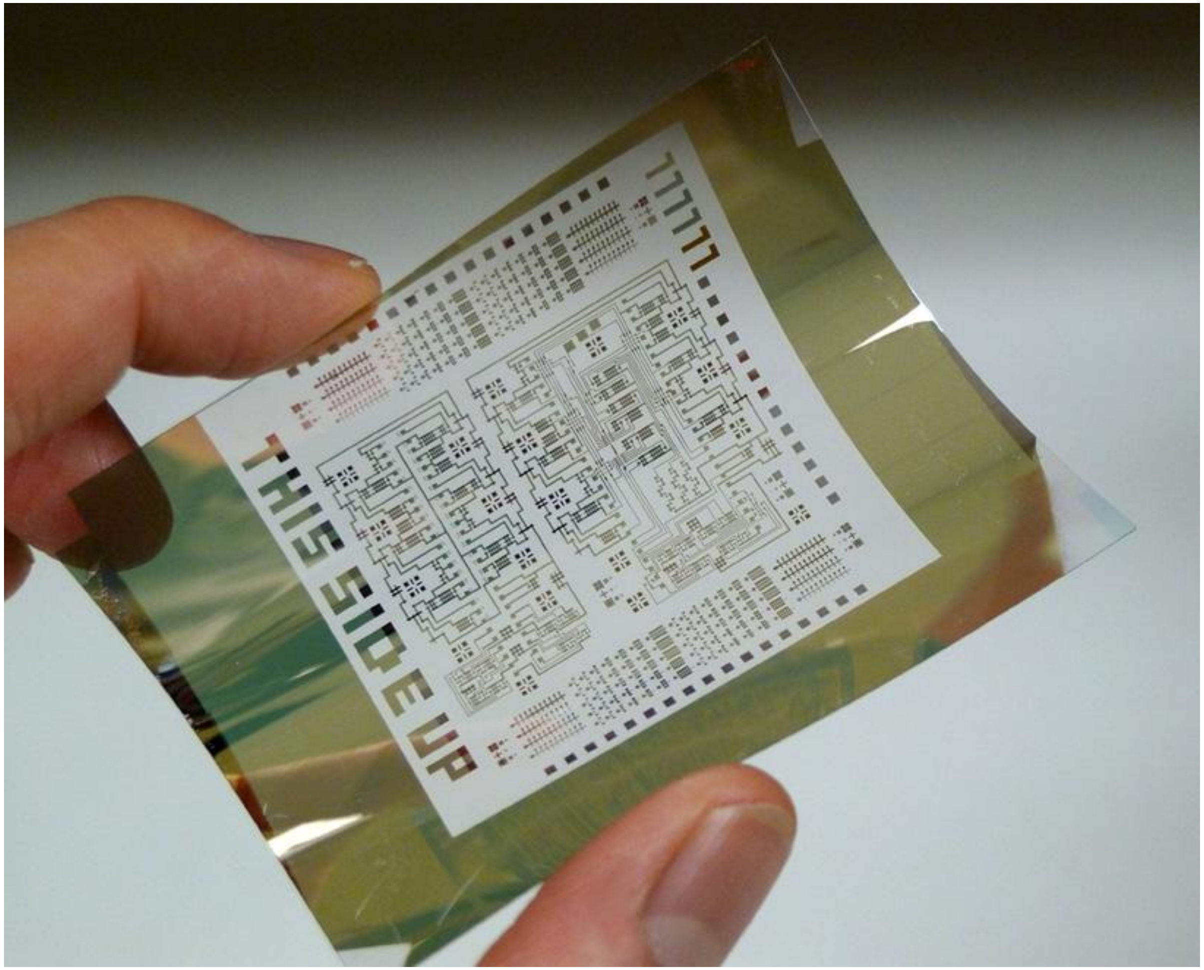
http://muri.mse.vt.edu/

Jellyfish Bell Prototype (Virginia Tech)

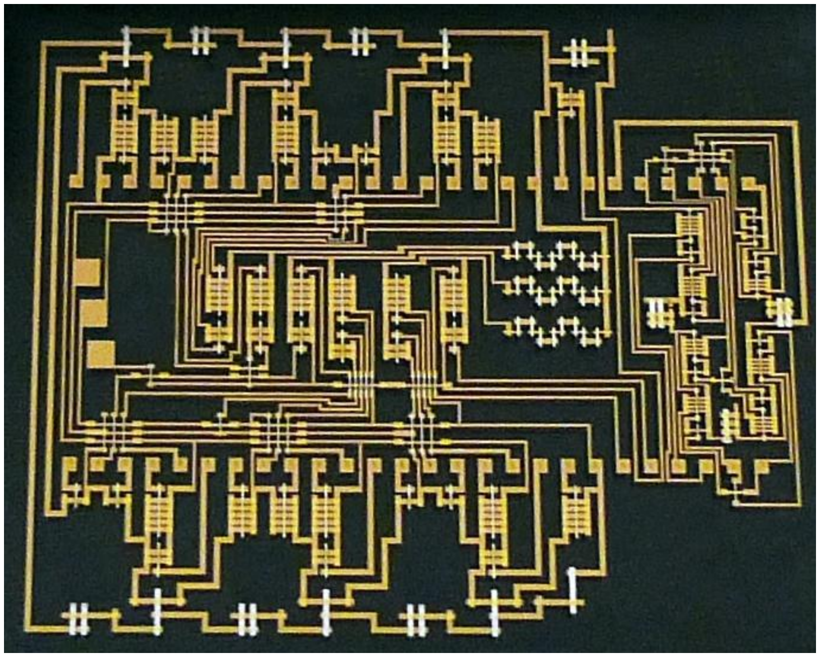


A bio-inspired shape memory alloy composite (BISMAC) actuator
A .A .Villanueva, *et al.*, 2010 *Smart Mater. Struct.* **19** 025013 (17pp)

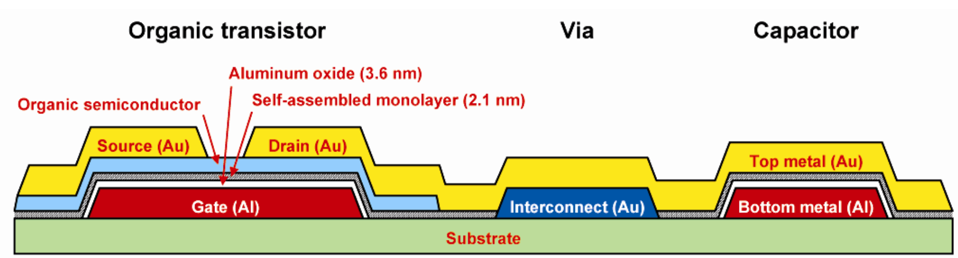
Want to Make Plastic ADCs !



6-bit A/D Converter Prototype

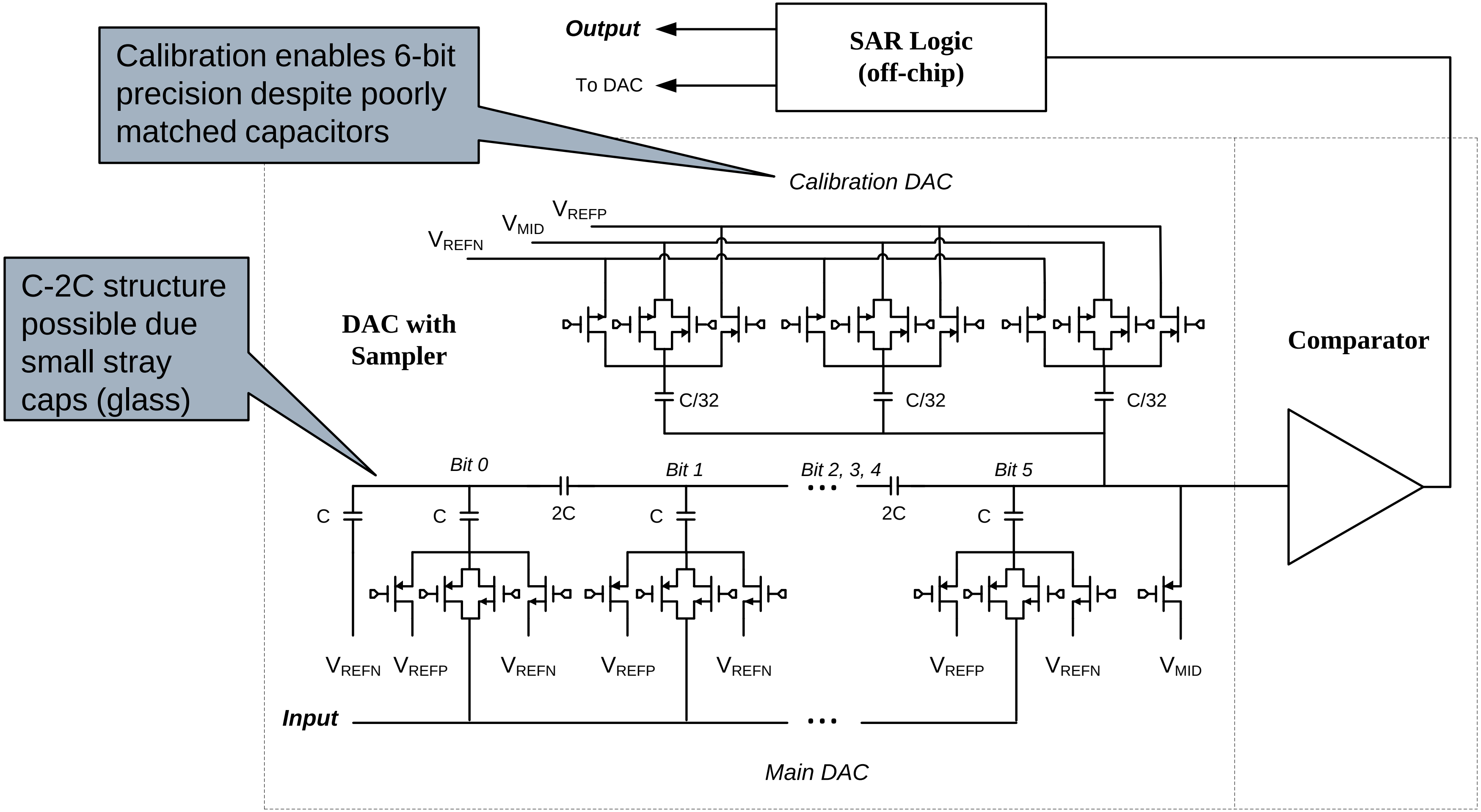


Substrate	Glass
Interconnect	Ti/Au evaporation, litho, wet etch
Gate electrodes	Al evaporation, shadow masking
Source/Drain	Au Evaporation, shadow masking
Dielectric	5.7nm AlO_x/SAM
PFET	DNTT, ~0.5 cm^2/Vs
NFET	$F_{16}CuPc$, ~0.02 cm^2/Vs
Area	28mm x 22mm
Component count	74



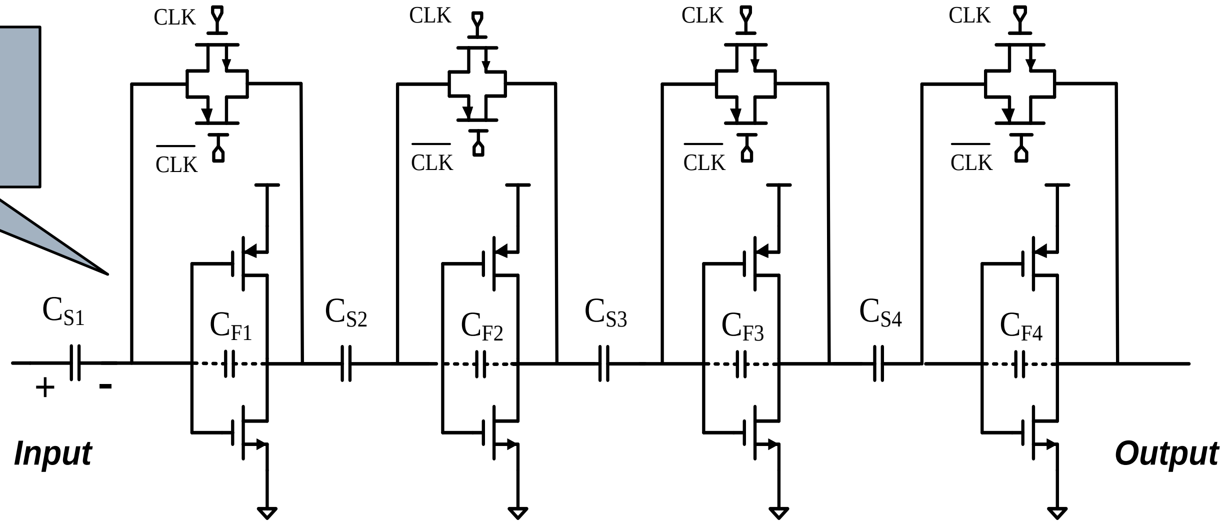
W. Xiong, U. Zschieschang, H. Klauk, and B. Murmann, “A 3V, 6b Successive Approximation ADC using Complementary Organic Thin-Film Transistors on Glass,” ISSCC 2010.

ADC Schematic

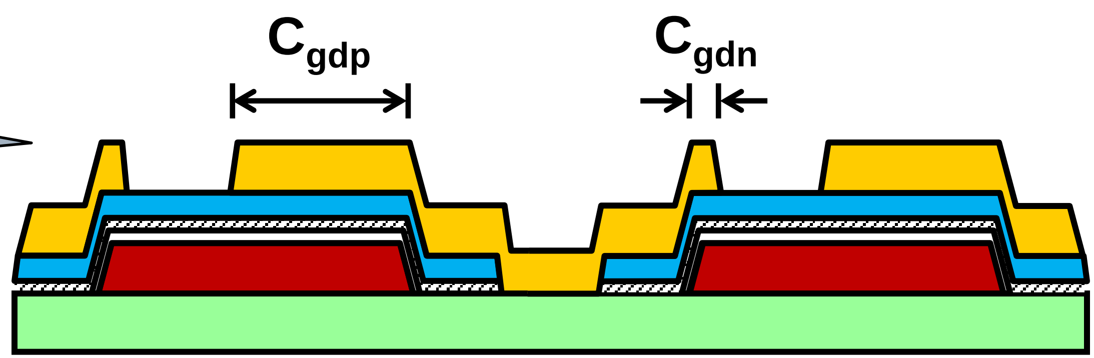


Comparator

Auto-zeroing cancels threshold voltage drift

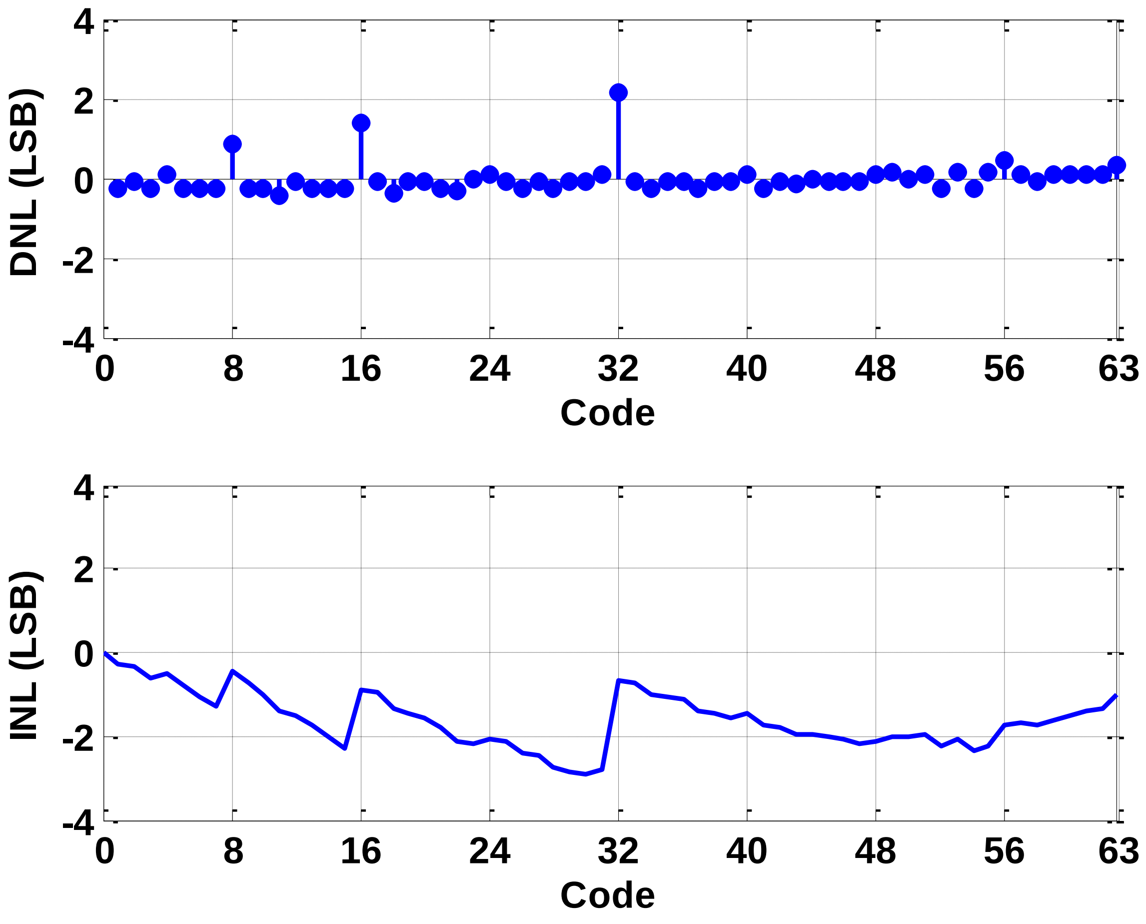


Anti-parallel PFET/NFET layout minimizes variations if C_F due to misalignment



Measured DNL/INL

Before calibration, 100 Hz clock rate



Measured DNL/INL

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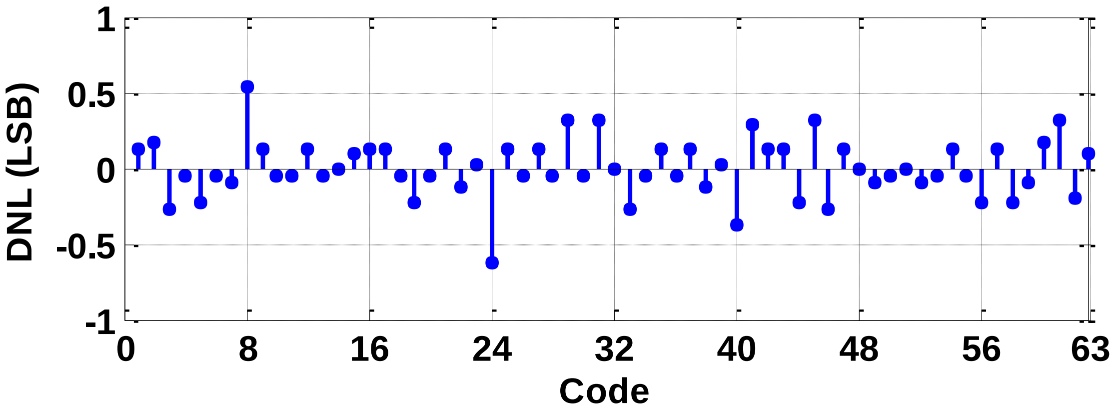

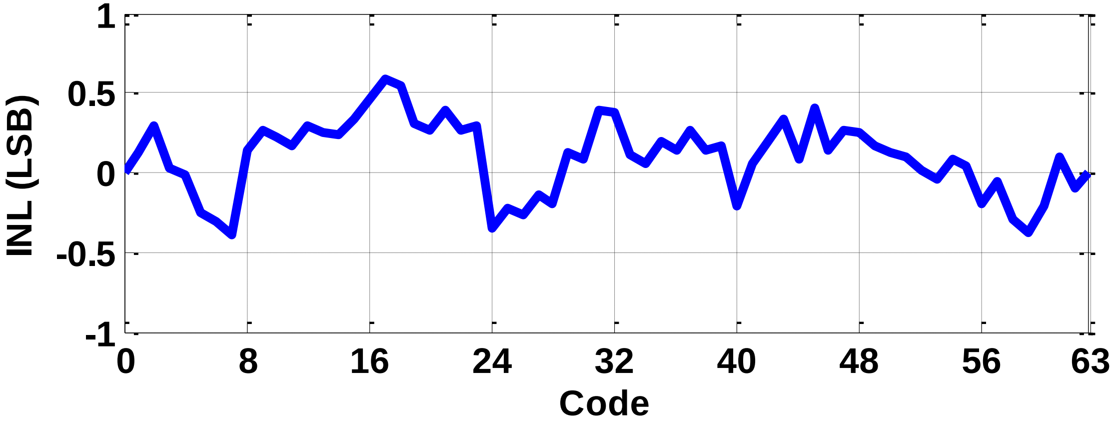

Organic ADC Summary

Process	3 metal complementary organic thin-film
Minimum feature size	20 μm
Chip area	28 mm x 22 mm
Resolution	6 bits
Full-scale range	2 V
Max DNL / INL	-0.6 LSB / 0.6 LSB
Clock rate / Update rate	100 Hz / 16.7 Hz
Power consumption	3.6 μW @ 3 V

Conclusions

- Mixed-signal IC design remains a vibrant area of research
- Changing boundary conditions
  - Ever-increasing need for higher performance, lower power
  - New applications
  - New device technologies
- A recurring theme in our research
  - Looking for new ways to overcome analog imperfections using DSP and calibration